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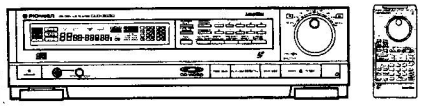
Service Manual



SERVICE GUIDE
ORDER NO.
ARP 1560

CD CDV LD PLAYER

CLD-3030

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1. FOCUS (FOCS), TRACKING (TRKG), SLIDER (SLDR) AND TILT SERVOS (DESCRIPTION OF THE HA11529).

1.1. SUMMARY

The HA11529 is an analog/digital hybrid bipolar IC which performs the following functions:

1. FOCS servo control (FOCS servo loop pull in control, FOCS servo loop gain control)
2. TRKG servo control (TRKG servo loop ON/OFF and brake control during track jump and SCAN operations)
3. SLDR servo control (SLDR servo loop ON/OFF, variable speed transport, motor PWM drive)
4. TILT servo control (TILT servo loop ON/OFF)
5. CD/LD FOCS and TRKG servo switch
6. All of the above functions are controlled by 8-bit serial data passed through a serial bus (DATA, CLK, LATCH).
   The 8-bit serial data commands are as shown below.

MODE	ADDRESS DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
SCAN MODE CONT	1	0	0	0	SCAN SPEED 1	SCAN SPEED 2	SCAN SPEED 3	1: SCAN ON 2: SCAN OFF
SERVO CONTROL 1	1	0	0	1	FOCS 1: ON 0: OFF	DIRECTION 1: FWD 0: RVS	TILT 1: ON 0: OFF	1: LD 0: CD
SERVO MODE CONTROL 2	1	0	1	0	TRKG Zero cross output 1: 1/256 0: Through	TRKG 1: OFF 0: ON	TEST 1: TEST 0: NORMAL	—

* It is possible to set SCAN SPEED at 7 stages using the 3 bits, D3/D2/D1.

1.2. HA11529 Pin Functions

Pin No.	Pin Function
1.	Vee: −5V
2.	FOCS ERROR signal input: OP AMP input to which a SW is connected for gain control during SCAN
3.	FOCS SUM input: For DISC detection. Comparator input threshold is +0.4V.
4.	Comparator input threshold for the FOCS S-curve detection is +0.3V.
5.	Comparator input threshold for MAIN BEAM ON/OFF track detection is +0.5V. FOCS SUM input.
6.	TRKG ERROR input: Comparator input threshold for TRKG ERROR zero cross detection is 0V.
7.	GND
8.	TRKG ERROR AMP for CD input
9.	TRKG ERROR AMP for LD input
10.	TRKG ERROR AMP output. TRKG servo phase compensation is connected between this pin and pins 8, 9.
11.	Output for switching the TRKG servo loop characteristics during track jump.
12.	Outputs the actuator drive and brake pulse during track jump and the actuator brake pulse during SCAN.
13.	Window comparator input to detect the amount of movement in the TRKG actuator during SCAN. Threshold voltage is 0.2V. Actually, an FTS SCAN signal is being input.
14.	Current setting terminal for TRKG actuator brake.
15.	Current setting terminal for pins other than 14P
16.	TRKG RTN input: TRKG RTN input for SLDR servo.
17.	SLDR servo amp output: During play, the SLDR motor is PWM driven and at that time this pin becomes the window comparator input.
18.	SLDR drive signal output during play or when high speed slider is in operation.
19.	SLDR drive signal input when SLDR is operating at low or mid speeds.
20.	Capacitor connected pin for setting the slope of the reference triangular wave for the SLDR motor PWM drive during play.
21.	Resistor-connected pin to set comparator threshold for turning off the TILT servo drive.
22.	TILT ERROR input: op amp input.
23.	A VR is connected for setting the TILT servo gain with the output of the op amp from 22P.
24.	Output for TILT motor drive.
25.	T-CROSS output: TRKG ERROR zero cross count output. Depending on the serial data command, output may be divided by 256.
26.	F-LOCK: L when FOCS lock activated.
27.	J-TRIG input: triggered at startup. L under normal operating conditions.
28.	RESET input:
29.	LATCH input: serial interface bus to the system microprocessor CPU. (29, 30, 31P) Data is latched on the trailing edge.
30.	SDATA input: 8-bit serial command data input.
31.	SCLK input: clock for serial data transmission.
32.	500kHz input: internal logic clock input.
33.	TEST pin: normal state = L.
34.	Pin for setting the injection current used by internal I2L logic.
35.	Capacitor connected pin for setting the lens UP/DOWN cycle when FOCS ON is activated.
36.	Drive voltage output for lens UP/DOWN.
37.	FOCS Error amp output: FOCS servo phase compensation is connected between 38, 39P.
38.	FOCS Error LD input.
39.	FOCS Error CD input.
40.	Pin with connected offset adjustment VR that uses the uninverted FOCS Error amp input
41.	Op amp output for FOCS gain control
42.	Vcc: +5V.

1.3. DESCRIPTION OF FUNCTIONS

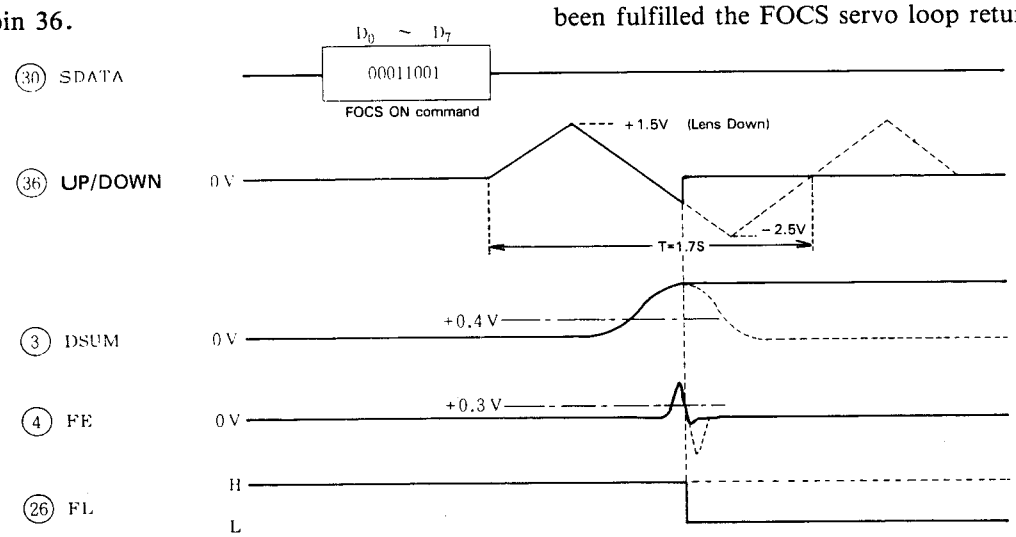
1.3.1. FOCS Assembly

1) FOCS pull in operation

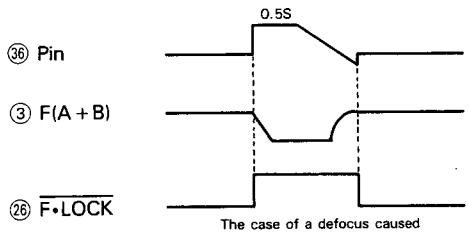
The pull in operation of the FOCS servo raises the objective lens UP/DOWN and, when the input of DSUM (pin ③) and FE (pin ④) fulfill FOCS lock conditions, turns the FOCS servo loop ON. In the case of a defocus caused by damaged disc, the FOCS servo loop is turned OFF and, about 0.5 seconds later, a voltage of +0.6V is output at pin 36.

2) FOCS down and repeat pull in

When the input of DSUM (pin ③) falls below +0.4V as a result of a damaged disc or excessive external vibration, the unit detects an abnormal condition. When this occurs the FOCS servo loop is turned off and at the same time the objective lens is automatically moved UP/DOWN. When conditions as described in 1) have been fulfilled the FOCS servo loop returns to ON.



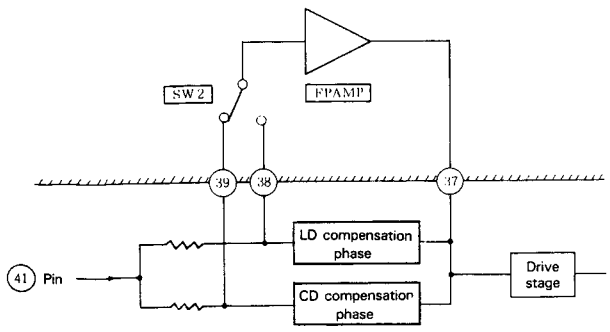
* The dotted line indicates the wave form when the FOCS loop is not ON.



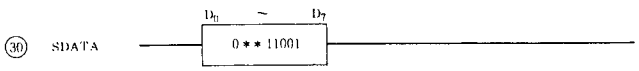
The case of a defocus caused

3) CD/LD switching

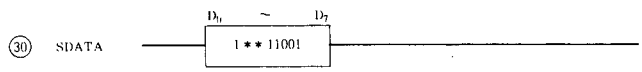
Depending on what type of disc is being played, compact disc or laser disc (CD or LD), a switch alters the loop gain and phase compensation of the FOCS servo for the particular disc type. The serial data bit for the CD/LD switch has the same address as the FOCS ON command bit and both can be set with a single transmission.



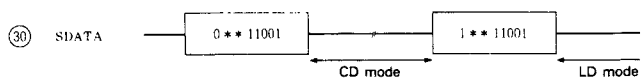
i) Focus ON command when the CD mode is set.



ii) FOCS ON command when the LD mode is set.



iii) When the CD/LD mode is switched in the middle of playback (CD mode → LD mode)



Note 1) The asterisks (*) represent bits which bear no relation to the operation under examination. (This convention will be used throughout the manual.)

1.3.2. TRKG Assembly

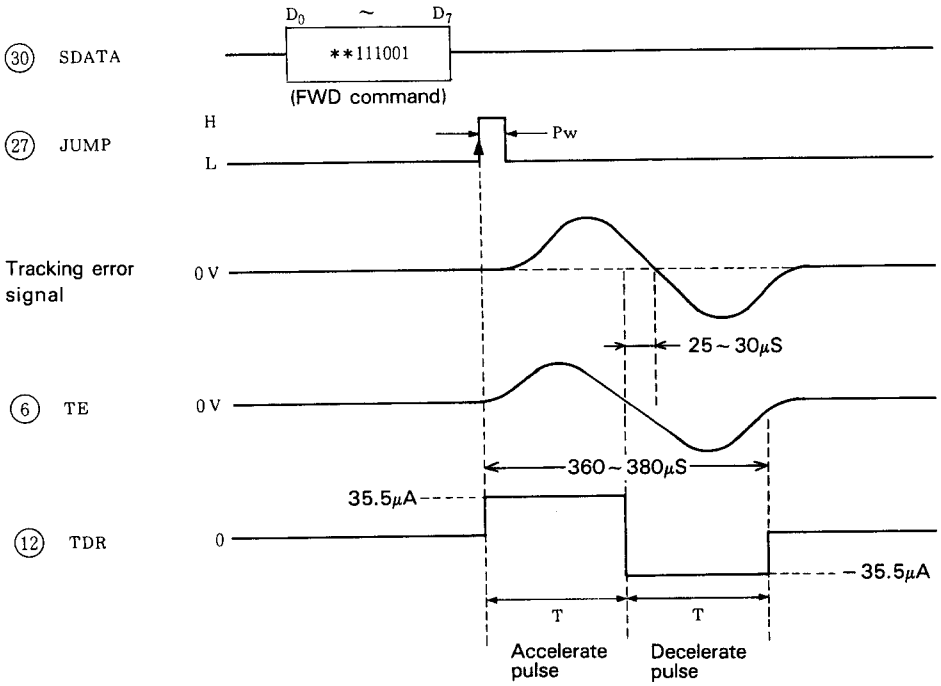
1) Track jump operation

Track jump commences when the jump trigger start-up pulse is received from JUMP (pin ㉗). Acceleration and deceleration switching are performed by monitoring tracking error zero cross. During a jump operation, SW12 and SW24 are activated sequentially. SW12 is used to switch TRKG loop characteristics and SW24 for adjusting the position of TRKG error zero cross.

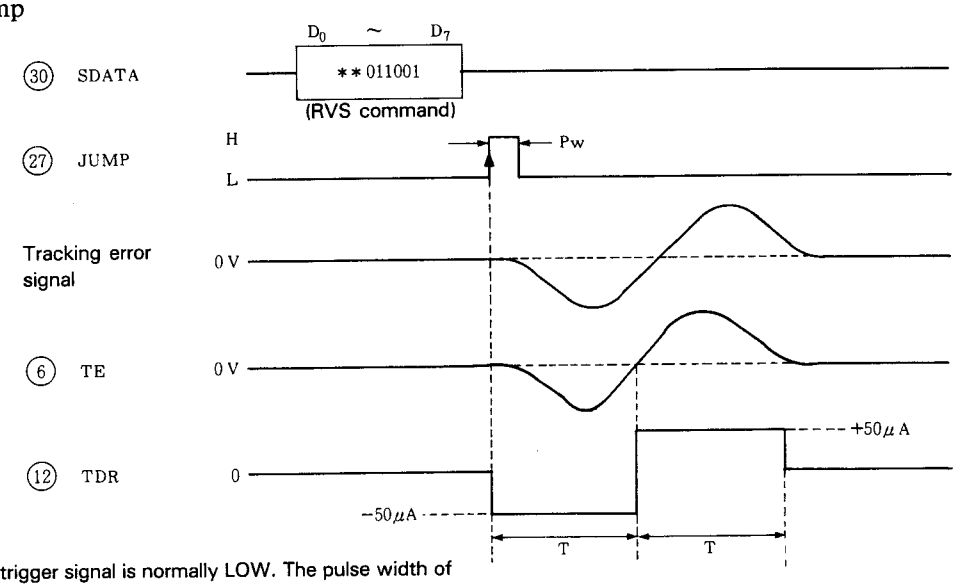
Switching between forward and reverse jump is performed by serial data transmission.

The jump trigger signal, by turning Q17 OFF only during a jump, cuts off C54 to which 6P is connected so that the phase of the input signal to 6P can be pushed forward beyond its position during normal operation.

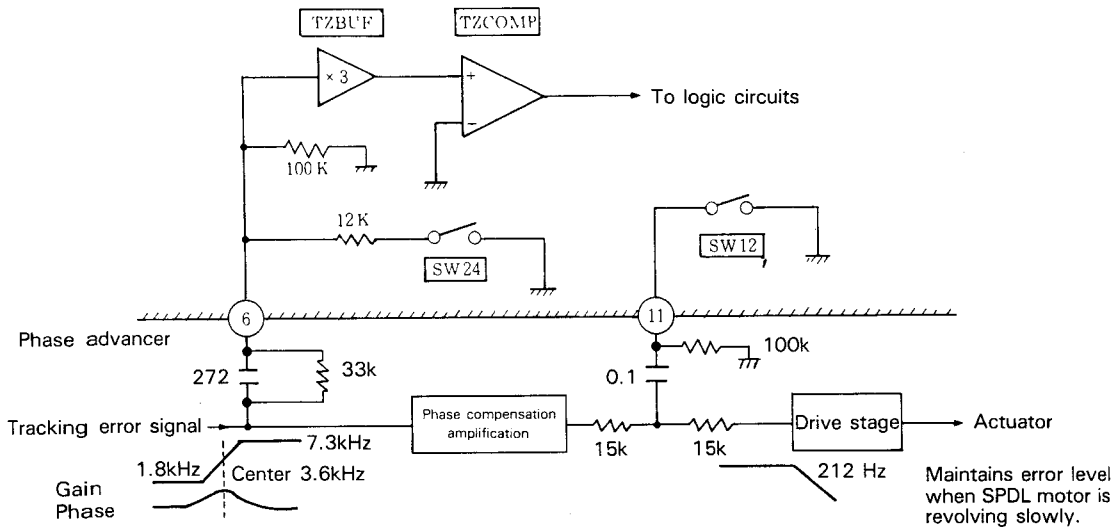
i) Forward jump



ii) Reverse jump



Note 1) The jump trigger signal is normally LOW. The pulse width of Pw is set at 9.6μS.



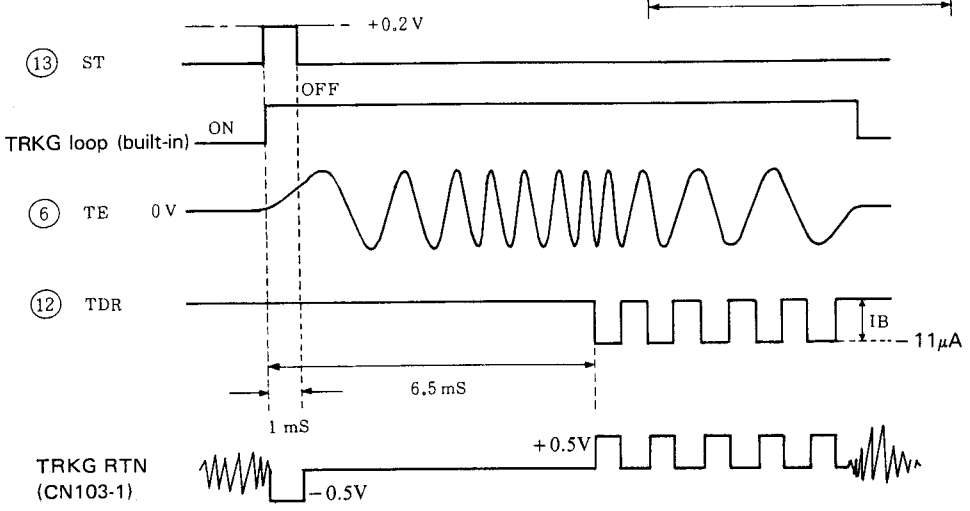
2) Scan operation

During slow or medium scan the TRKG servo performs ON/OFF control of the TRKG loop. Input to ST (pin ⑬) signals displacement of the actuator position and the TRKG loop is turned OFF. When the error signal at TE (pin ⑥) drops below a set frequency, the TRKG loop is turned back ON.

While the TRKG loop is OFF, a brake pulse is output by TDR (pin ⑫) according to the timing charts shown below. The polarity of the brake pulse is not a direction command sent via serial data but is determined by the polarity of the signal input to ST (pin ⑬). Corresponding to actuator speed as detected by TE (pin ⑥), brake pulse duty is automatically set to operate in 5 stages (50%-100%). Brake current IB can be adjusted at BSET (pin ⑭).

Because switch timing for the open/close operation of the TRKG servo loop during SCAN is determined by the system microprocessor, an FTS signal like that shown below is actually input to pin ⑬.

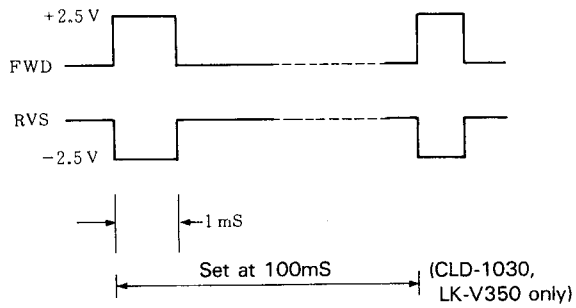
i) Forward scan



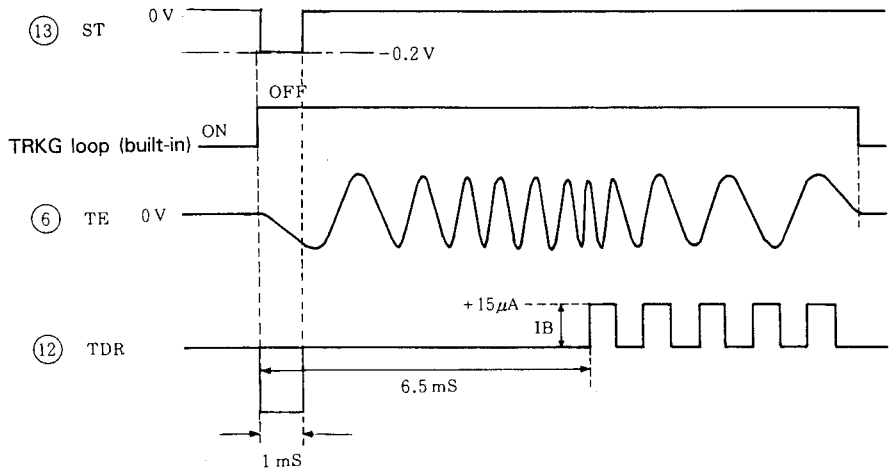
This signal also flows into pin ⑫, but the polarity of the brake pulse is opposite to it, which acts to improve convergence during braking.

The cycle of the FTS SCAN signal varies depending on the absence or presence of video memory.

1) The CLD-3030 (with video memory)
   After a jump, the TRKG servo loop closes and if one field worth of data has been properly written to memory, the following FTS scan signal is output. To account for possible mistakes in writing to memory, the period for this operation is not fixed.
2) CLD-1030, LK-V350
   The period is set at 100mS.

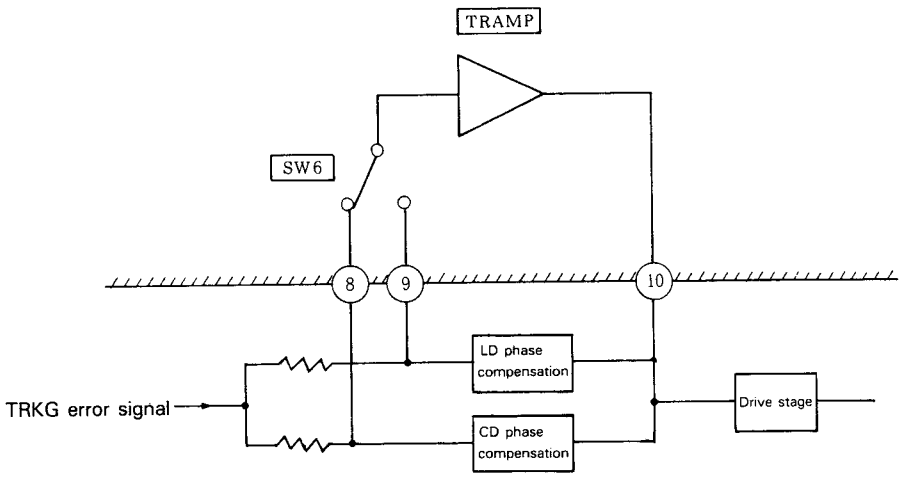


ii) Reverse scan



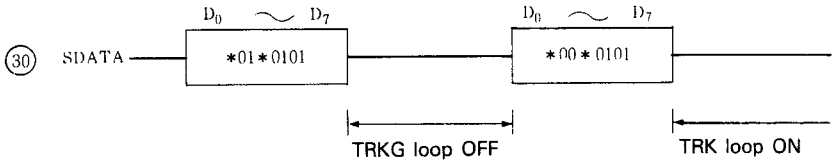
3) CD/LD switching

Switching between CD and LD is performed in exactly the same way as CD/LD switching for the FOCS servo.



4) TRKG loop ON/OFF control

Switching the TRKG loop ON/OFF is done by means of serial data transmission.



5) TRKG count

The number of tracks crossed during high speed scan is counted and then, according to the serial data transmission, a choice is made to either divide (1/256) the output TCNT (pin ㉕) pulse or output it as is.

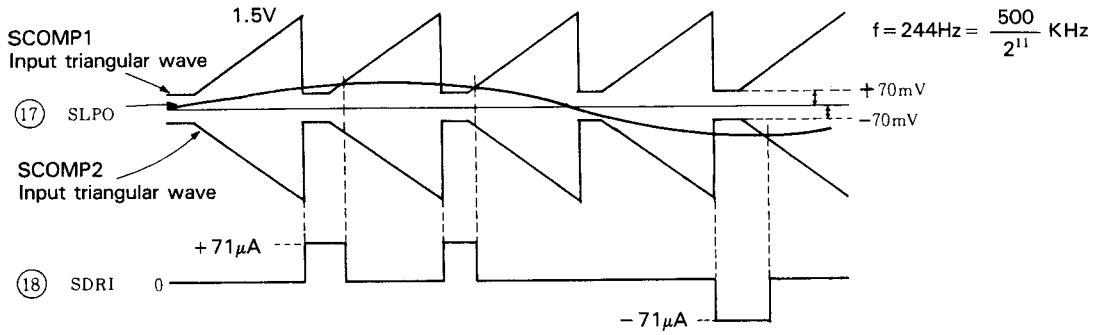
When a misclamp is detected at the beginning of play, the pulse is divided (1/256) and when tracks are counted during CD search the pulse is output as is.

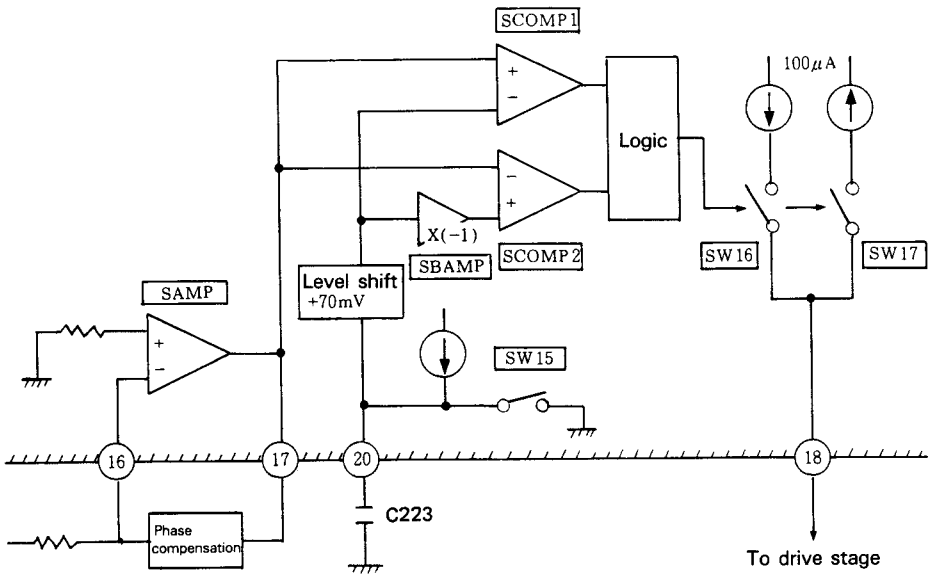
Once play has begun and the TRKG servo loop is open, track crossing is normal if the number of tracks crossed per disc rotation (6 FG pulses = 1 rotation) is under 1,280 tracks (TRKG count, 5 times: 1mm of eccentricity). If this number is exceeded, however, a misclamp is detected and the disc is ejected from the unit.

1.3.3. Slider Assembly

1) Operation in the normal play mode

During normal play DC components in the drive current of the TRKG actuator are PWM modulated at SCOMP1 and SCOMP2. This PWM pulse turns SW16 and SW17 ON and activates the output of the drive signal. The slope of the reference triangular wave can be altered by means of the capacitor connected to SLP (pin ⑳).



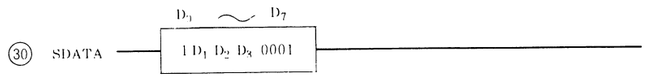


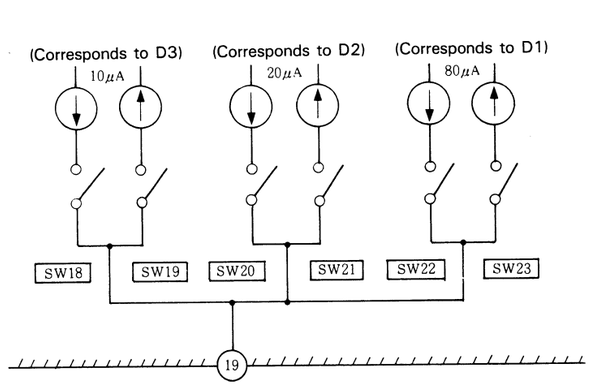
2) Operation in the scan mode

During a scan operation, the SLDR servo loop is OFF and a signal that agrees with the set speed as given by serial data transmission is output either from SDR2 (pin ⑲) or SDR1 (pin ⑱).

i) Low and mid speed scan

SW18, SW20 and SW22 (when set in the FWD direction) or SW19, SW21 and SW23 (when set in the RVS direction) correspond to the serial data, D3, D2 and D1. When the bit is "0", it is OFF, and when the bit is "1", it is ON. Furthermore, on the basis of these three bit combinations a current of 10μA — 110μA (FWD) or −10μA — −110μA (RVS) is output as a duty 50% pulse from SDR2 (pin ⑲). Actually, however, when the unit is used as a CD player, only ±110μA is used.

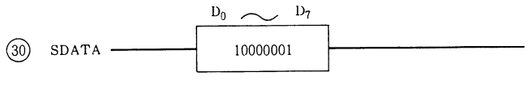




ii) High speed scan

By means of the serial data transmission shown at the right, SW16 or SW17 can be turned ON and a ±110μA drive signal output from SDR1 (pin ⑱). The direction is as given in the serial data transmission.

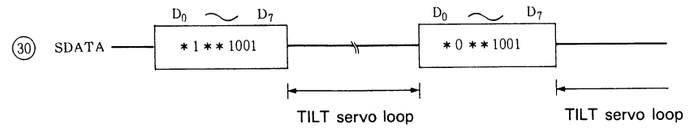
When the unit is used as an LD, the SCAN SPEED control function discussed above is not employed. A combination of the two commands, 10000001 for high speed SCAN and 10001110 that turns the SLDR servo loop OFF are used to control SLDR drive voltage and set SCAN SPEED.



1.3.4. TILT Assembly

1) Loop ON/OFF switch

The ON/OFF control of the TILT servo loop is performed by means of serial data transmission.

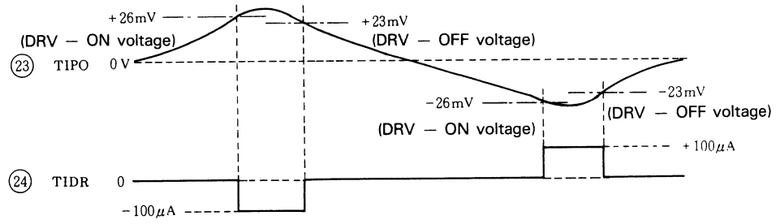


2) TILT servo operation

The TILT error signal is input to the window comparators TCOMP1 and TCOMP2. The drive voltage which is output at TSEF (pin ㉑) operates on an ON/OFF basis.

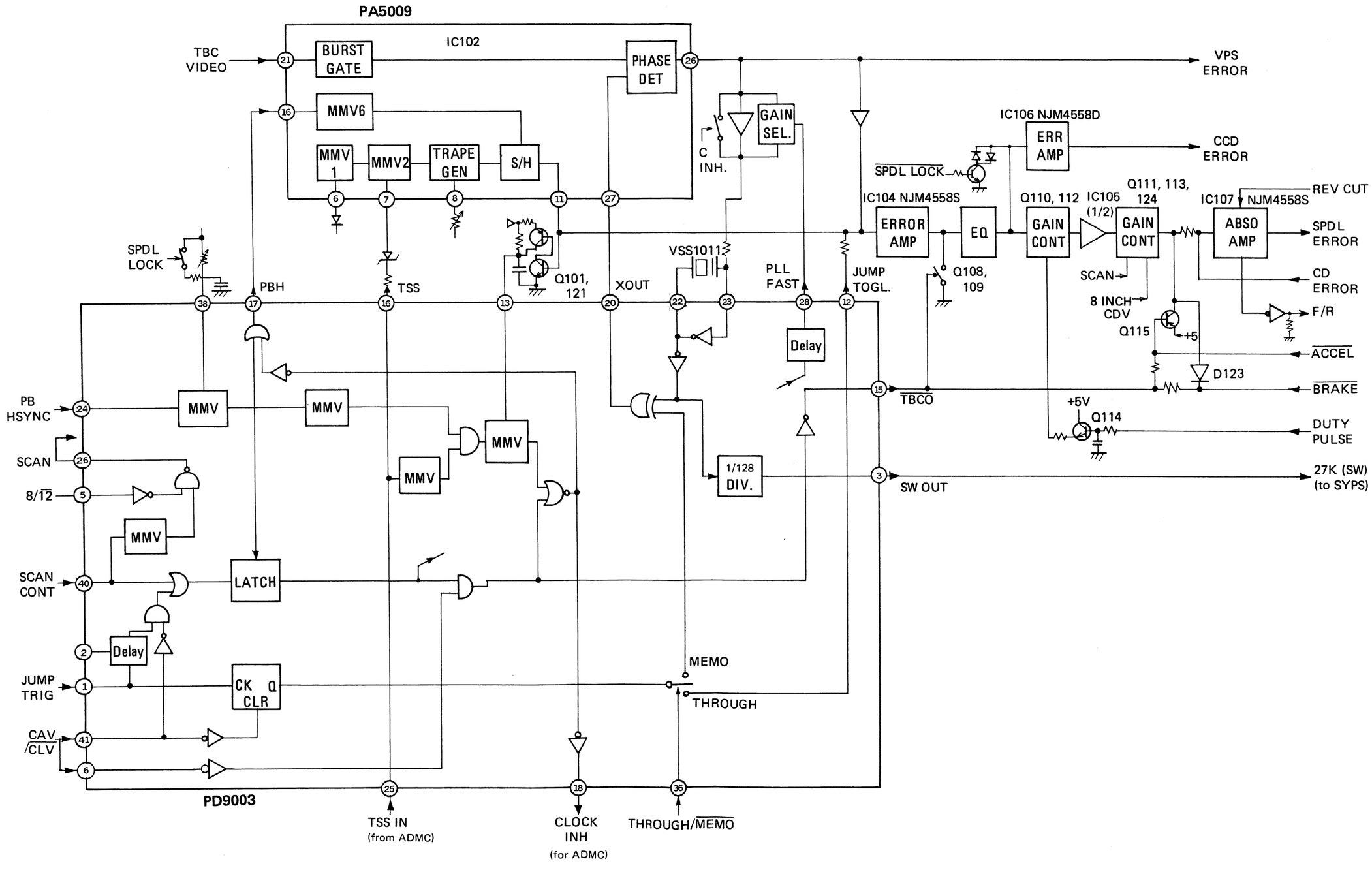
If input is higher than the TCOMP2 reference voltage (DRV — ON voltage), then ON; if input is lower than the TCOMP1 reference voltage (DRV — OFF voltage), then OFF.

DRV — OFF voltage can be adjusted at TSEF (pin ㉑).

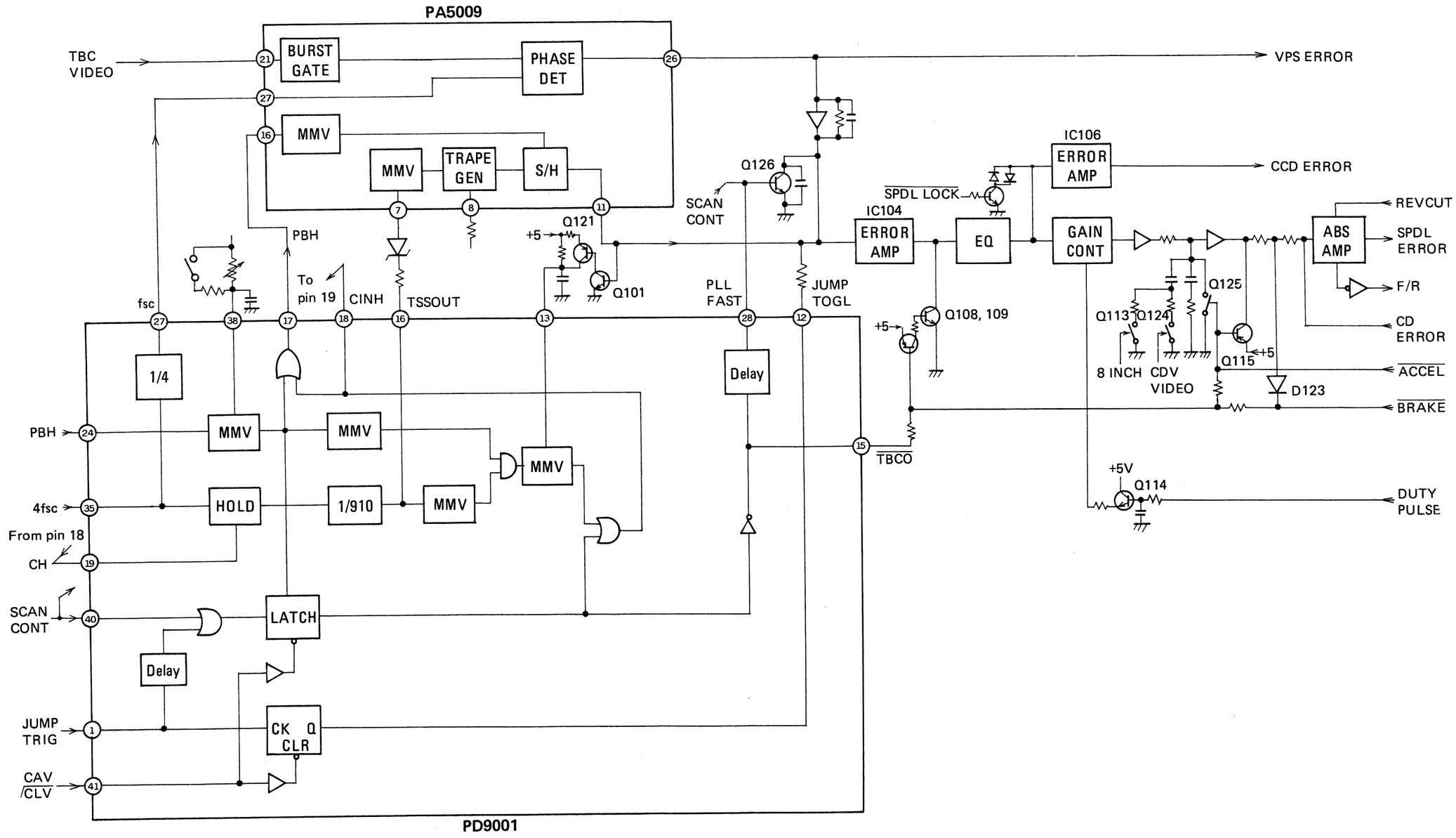


2. SPDL SERVO AND TBC (TIME BASE CORRECTOR)

2.1. VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-3030)



2.2. VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-1030, LK-V350)



2.3. DESCRIPTION OF VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-3030)

Comparison error between the trapezoid derived from the TSS signal (576fH/576) and PB-H (Playback H-synch) is output by IC102-11P (PA5009) and amplified by error amp IC104 (NJM4558S).

IC106 is the CCD error amp. After the SPDL servo lock is ON, Q123 becomes an error limiter. Q110 and 112 are variable gain amps and, as the collector voltage to Q110 rises, GAIN is lowered.

During CLV disc play, Q114 smooths out the duty pulse which is output by the system microprocessor CPU for SPDL servo loop gain control.

Q111 and 116 are GAIN switches during scan. Q113 and 124 are gain switches for 8INCH disc play and CDV disc play, respectively.

- **VPS (Video Phase Shift)**

VPS error is derived by phase shift comparison between PB-B (Playback-Burst) at IC102 and the output of 3.58M VCXO near 23 Pin, IC101 — 22 Pin.

Error output from IC102 - 26 Pin is input to the error amp of IC103 (1/2).

Gain switches Q104 and 105 have been added to IC103. When Q104 is OFF, error detection loop gain increases and activates the FAST mode.

When Q104 is ON, gain is lowered and because the detection loop trails only the low frequency components, high frequency error components remain in the error output of 26 Pin. These are output as VPS error to the VSOP Assembly (VDEM section).

The switch into the FAST mode is performed by means of the PLL FAST signal from 28P which delays TBCO output from IC101 - 15P.

- **CD/CDV play**

The operation of CDV video play sections is exactly the same as for LD video play.

During the audio play sections of CD or CDV, CD SPDL error is input to the absolute value amp IC107 by board 4FSB (digital decoder) and the SPDL motor driven.

2.4. SUMMARY OF SPDL & TBC

	CLD-3030
SPDL error detection CCD/CPC error detection	} PD9003 + PA5009
SPDL REF-H	T.S.S. (regardless of memory ON/OFF)

Frequency phase errors and CCD errors are detected by using the trapezoid generated from REF-H (Reference-H-synch) and PB-H (Playback-H synch), as well as the method of reference shift which delays REF-H by either 28μsec or 36μsec when necessary. Furthermore, spindle and CCD servos are always operating at the same time.

During SCAN and other operations, when the TRKG servo loop is open, REF-H is being held. And when the servo loop is closed, REF-H is activated in phase with PB-H. The fact that SPDL and CCD servos are turned on at the same time after a jump, with the CCD servo operating until the SPDL motor has been able to absorb frequency component errors, allows the color lock to be activated immediately after a jump.

Consequently, in the CLD-3030, since the TSS signal, which is the 576fH, A/D, D/A conversion clock of the video memory section, undergoes frequency division by 576 at PDJ002, is being employed, memory ON/OFF no longer has any bearing on the status of REF-H. In the CLD-3030, the ICs employed for SPDL servo detection and for CCD and CPC error detection are PD9003 and PA5009. The CLD-1030 and LK-V350 employ PD9001 and PA5009.

<Deleted features>
1. 910 dividing circuit and REF-H switch
2. 8/12 INCH recognition

<Added features>
1. 3.58MHz VCXO output is divided and a 27kHz signal generated for the SPDL motor PWM (formerly 2fH).
2. SPDL GAIN switch timing is derived from the SCAN CONT signal.

SPDL/CCD error detection, 3.58MHz VCXO, and JUMP TRIG signal processing sections are the same as the PD9001 and pin numbers and names for these sections have remained the same as well.

Because in the CLD-1030 and LK-V350, which have no video memory, there is no TSS signal either, it is necessary to frequency divide 4fsc by 910 for REF-H.

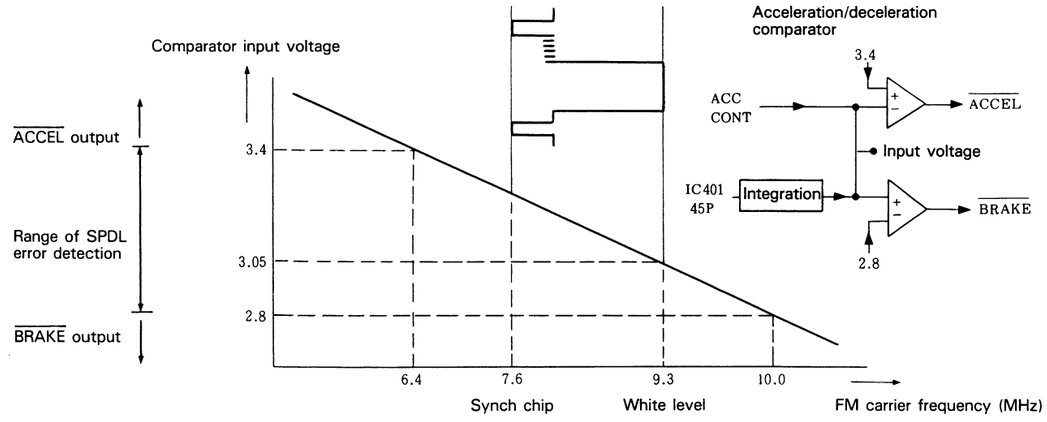
2.5 DETECTION AND CONTROL OF RUNAWAY SPDL MOTOR

In cases where the SPDL motor runs out of control, i.e., if the SPDL motor rpms for whatever reason get out of the servo's tracking range, speed can be controlled by using either acceleration (ACCEL) or deceleration (BRAKE) signals.

In this manual, voltage inversely proportional to the video FM carrier frequency in the RF signal from the screen image demodulation section is extracted and input to the acceleration/deceleration signal detection comparator.

The output of IC401 (PA5010) — 45P of the VSOP Assembly (VDEM, ADEM) is integrated and input to the comparator of IC403 (NJM2903). The input voltage to the comparator is as shown in the figure below.

When the FM carrier frequency is at the 100% white level, equivalent to 9.3M, the comparator input voltage is at 3.05V. The upper and lower threshold voltage levels are then set at the detection limits of the SPDL servo frequency error. The ACCEL signal is over 3.4V and the BRAKE signal is under 2.8V. Both are labeled L.



Detection works on the basis of DC voltage when the SPDL servo LOCK goes out of order and rotational speed is thrown off. ACCEL or BRAKE signals are output when disc speed goes beyond the tracking range of the servo. These oblige the spindle motor to accelerate or decelerate until rotational speed again falls within the range of servo control.

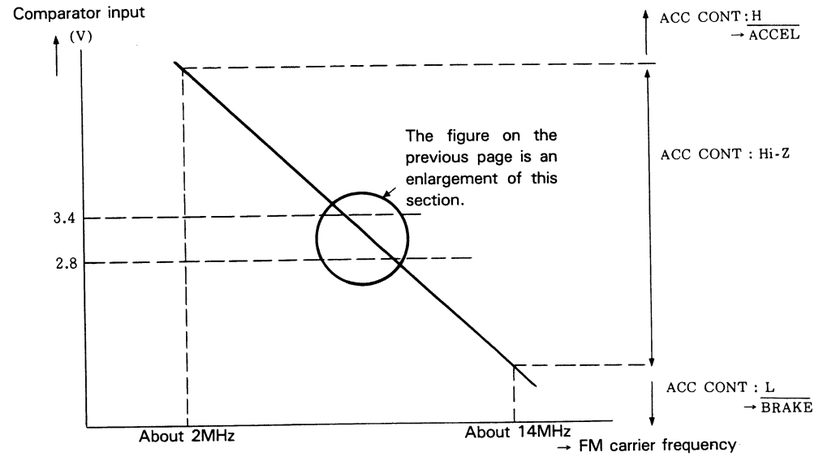
When the outer tracks of a CLV disc are being played and the SPDL motor is rotating relatively slowly, it may be possible, if the SPDL servo is locked, to detect acceleration or deceleration signals being used to maintain the FM carrier frequency within the range shown in the figure above.

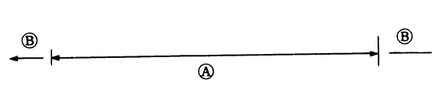
However, if the LOCK goes out of order and SPDL motor rotation is radically disrupted, the relation between frequency and DC voltage becomes non-linear and detection is no longer possible.

For this reason, the FG output cycle of the SPDL motor is measured by the system microprocessor CPU. If it falls into the areas marked B in the figure below, i.e., beyond 80% of reference speed, ACC CONT (ACCEL CONTROL) which is input to the acceleration/deceleration comparator registers either H or L and SPDL motor speed control is performed by the CPU.

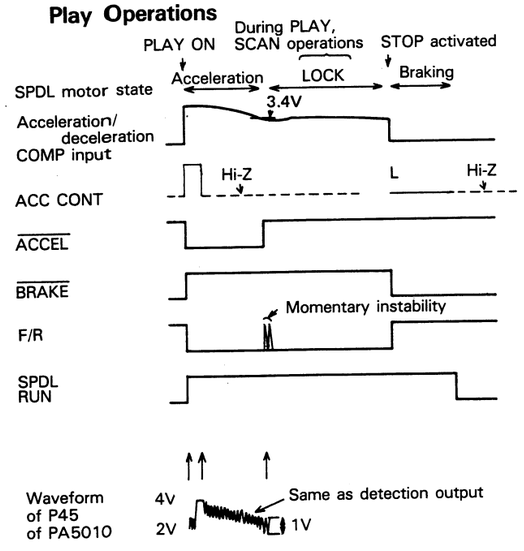
In addition, the system microprocessor CPU also performs SPDL motor stop detection at the conclusion of play based on the FG output cycle.

When rotational speed is within 80% of reference speed (the area marked off as A in the figure below), the ACC CONT signal is in a Hi-Z state and speed control is not performed by the CPU.





2.6 CLD-3030 SPDL Servo Timing Chart during LD Play Operations



Control Signals for SPDL Servo Timing

$\overline{ACCEL}$, $\overline{BRAKE}$: Output of the acceleration/deceleration comparator. The (3-state) ACC CONT signal from the system microprocessor CPU and the signal from 45P of PA5010 are integrate and input in the acceleration/deceleration comparator. The COMP input voltage in the Figure is derived from the sum of these two inputs.

$\overline{F}$/R : The signal at Q117, 118 which detects the polarity of the voltage going to the SPDL error absolute value amp in the SPDL servo circuit. This is input to the motor control IC on the BLDB board.

SPDL RUN : This is input to the motor control IC from the system microprocessor CPU. At SPDL start up, this becomes H along with ACC CONT. Later, this returns to L when the brake is released. (During rotation it is always H.)

< SPDL Start up Operation >

After FOCUS is locked, the system microprocessor CPU switches ACC CONT and SPDL RUN to H. When ACC CONT is H and $\overline{ACCEL}$ is L, Q115 is ON. This applies a positive voltage to the absolute value AMP (IC107) and about −1.5V is input as SPDL error to the SPDL drive circuit of SYPS assembly. At the same time, with Q117, 118 OFF, the $\overline{F}$/R signal shifts to L.

At this point, the configuration, SPDL RUN → L, $\overline{F}$/R → L, SPDL error → about −1.5V, triggers acceleration of the SPDL motor.

The system microprocessor CPU switches ACC CONT to Hi-Z when it detects that SPDL speed is within 80% of the reference value from the SPDL motor FG cycle.

Furthermore, the acceleration/deceleration comparator input is integrated at 45P of PA5010. At this point, with $\overline{ACCEL}$ at L and the application of DC 4V, acceleration of the SPDL motor continues.

As the SPDL motor accelerates, the acceleration/deceleration comparator input voltage drops. If it falls below the ACCEL threshold voltage, ACCEL switches to H and the SPDL/TBC servo loop closes.

When the loop closes, the SPDL servo performs reference shift and promptly locks.

<SPDL Brake Operation>

When the STOP or OPEN buttons are pressed, ACC CONT and $\overline{BRAKE}$ switch to L. Voltage is applied through D123 to the absolute value AMP (IC107), Q117, 118 shift to ON and $\overline{F}$/R shifts to H.

At this point, the configuration, SPDL RUN → H, $\overline{F}$/R → H and SPDL error → about −1.5V triggers application of the brake to the SPDL motor.

The system microprocessor CPU detects brake release timing from the FG cycle and shifts SPDL RUN to L and ACC CONT to Hi-Z to release the brake.

When FG is not input to the system microprocessor CPU, SPDL will continue accelerating from the onset as long as ACC CONT is maintained at H. Care should be taken at this point, because, if the OPEN button is pressed, the system microprocessor will judge that the SPDL has stopped, and regardless of whether it is rotating or not, will open the tray. Furthermore, when RF is not being input to PA5010, acceleration will stop at onset if ACC CONT shifts to Hi-Z and $\overline{ACCEL}$ to H. In this state, ACC CONT repeats H and Hi-Z and the SPDL continues rotating at low speed. (In one minute this state will be rejected.)

2.7. SPDL SERVO LOOP GAIN CONTROL DURING CLV DISC PLAY

A duty pulse with a duty ratio that is variable according to the disc time code is generated in the CPU, smoothed, and utilized for SPDL servo loop gain control.

The duty pulse has a 1V cycle with a sixteen stage variable duty ratio. The signal registers L at the innermost track and H at the outermost track. Providing the signal is smoothed, voltage will continue to rise as the pickup moves toward the outer tracks. This method derives a signal identical to that of obtained by slider resistor voltage and can perform the task of SPDL servo loop gain control during CLV disc play.

2.8. DIFFERENCES IN SPDL/TBC OPERATION DURING CAV AND CLV PLAYBACK

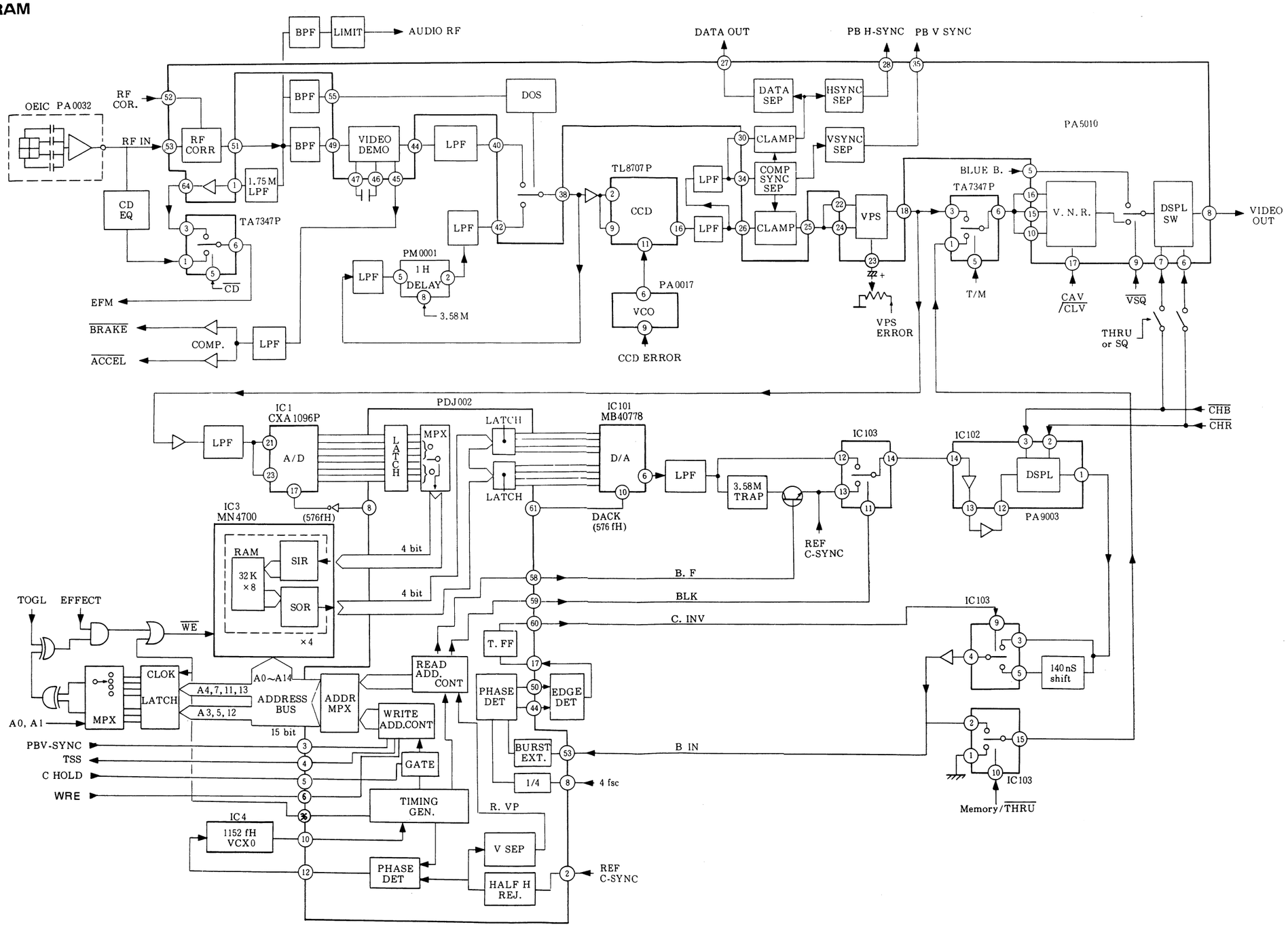
(○ : being output, X : not being output)

	< CAV >	< CLV >
During SCAN		
CLOCK INH	X	○
PLL FAST	○	○
TBCO	X	○
STILL, SLOW etc. (during track jump)		
CLOCK INH	X	○
PLL FAST	○	○
TBCO	X	○
JUMP TOGL	○ (memory-through only)	X

During CAV playback, even if the TRKG servo is open during SCAN, STILL and other operations, since CLOCK INH is not being input to the video memory section, reference shift is not being performed.

3. VIDEO SIGNAL PROCESSING SYSTEM (CLD-3030)

3.1. BLOCK DIAGRAM



3.2. SUMMARY OF VIDEO SIGNAL PROCESSING

The pickup of these models (1988 models) incorporates a unitized IC (PA0032) containing both photodetectors and head amp section. After gain adjustments have been made on the FTSB board, the output of PA0032 is input to the VDEM section of VSOP.

The flow of signals from the VDEM section and the operations of the various segments of the video signal processing circuitry are exactly the same as in the LD players. As can be seen from the block diagram, virtually all the indispensable circuitry is contained in the PA5010.

<PA5010 Functions>

- RF correction
- Video demodulation
- Dropout detection/Video correction SW
- EFM amp
- V-H synch and data separation
- VPS (Video Phase Shifter)
- VNR (Video Noise Reduction)
- Blue background SW and squelch
- Screen display
  (when video memory is OFF or when using blue background screen)

In other sections (for instance, CCD, CCD clock generating VCO IC, 1H delay IC), parts are identical to those used in the LD player.

The flow of signals in the video memory section is almost the same as in the LD-S1, although handling of the screen (character) display video in memory and through-video are two places where the '88 models operate differently.

With video that passes through memory, unless the characters are inserted before the 140nS shift circuit (equivalent to one half the cycle of the sub-carrier) that is used to maintain sub-carrier continuity between frames (every successive frame undergoes phase inversion), only the characters on screen will not be 140nS shifted.

3.3. SIGNAL PROCESSING IN THE VIDEO MEMORY SECTION

3.3.1. Signal Flow

The Video Memory Section is made up of two circuit boards: the ADMC and DAPS.

At the heart of the ADMC circuit board is the 1 M bit D-RAM and RAM control IC. It also includes those circuitry sections before the D/A converter.

The time axis corrected video signal is input to ADMC from the VDEM section of the VSOP board.

The IC1 (CXA1096P) is a parallel comparator type A/D converter and the A/D conversion reference voltage has been set at 26P (VRB pin) and 18P (VRT pin). The video signal level is shifted to coincide with the reference voltage, passed through an LPF (low pass filter) and then input to 21P and 23P. Reference voltage is 0 and-2V,and signals within that range undergo 8-bits A/D conversion.

The A/D conversion clock signal, which is set at 576fH (=9.06M) is input to IC1 — 17P from IC2 (PDJ002) — 80P.

The 8-bits data is divided at IC2 into an upper and lower 4-bits and transmitted in 4-bits form into memory. 1152fH VCXO is comprised of Q9, Q10 and IC4 (TC74HCU-04P) and is controlled at IC2 on the basis of error (output from IC2 — 12P) derived by phase comparison of REF-C-SYNC and memory READ address clock (READ REF-H). If the two signals are not phase locked, REF-C-SYNC insertion position and the D/A converted video signal will not coincide.

Writing to memory is indicated by a WE (WRITE ENABLE) signal from the system control.

A fixed time difference is maintained between write timing and memory readout timing, and the latter is always performed synchronously with REF-C-SYNC. Furthermore, unless a new frame is written to memory, the previous frame will continue to be output.

The DAPS circuit board contains the circuitry that follows D/A conversion. 8-bits data and the 576fH clock signal from IC2 are input to IC101 (MB40778) of DAPS.

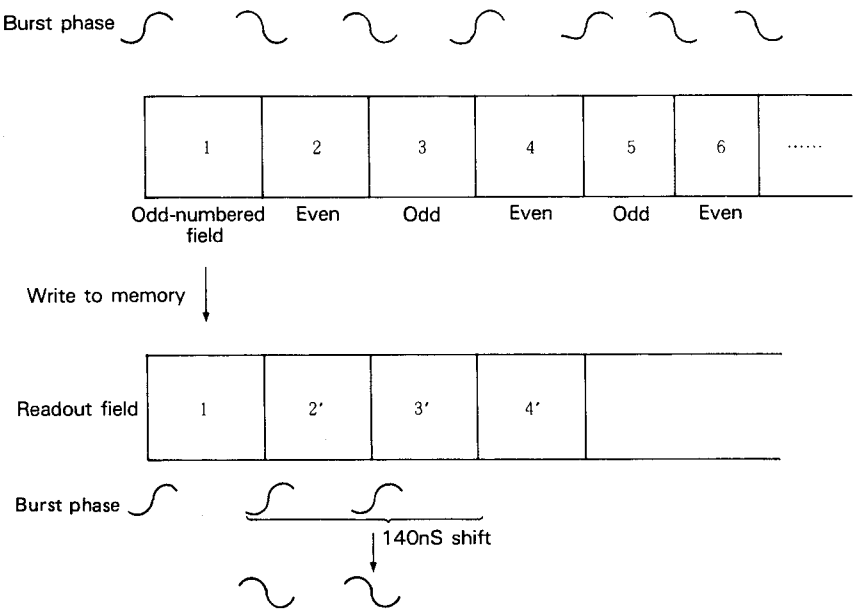
The IC101 D/A converter was also employed in the LD-S1, and the SYNC insertion, DSPL insertion and 140nS shift circuit occurring further downstream in the signal path are virtually identical to those found in the LD-S1 as well.

Insertion of the DSPL signal at DAPS is performed only for memory video. In the memory-through mode DSPL signal insertion is performed at PA5010 in the VDEM section of VSOP.

If DSPL signal insertion is performed in the VDEM section when memory is ON, dislocation occurs between the DSPL display and 140nS due to the fact that the memory video has been passed through the 140nS shift circuit. For this reason DSPL insertion must be performed before 140nS shift.

3.3.2. Necessity of the 140nS Shift

As the figure below shows, the burst phase of the NTSC video signal is reversed for each frame.



If by a still operation as shown above, field No. 1 is written to memory and then continuously read out, the burst phase for every field will become the same. In order to normalize the burst phase, the timing of fields 2' and 3' must be delayed for a period of time equal to one half the periodicity of the burst signal, or 140nS.

By delaying the video signal it is possible to perform an equivalent reversal of burst phase and thereby activate the color lock.

Detection of the discontinuous burst phase is done by comparing the 3.58MHz signal derived by frequency division of the reference clock 4fsc signal input from VSOP at IC2 (PDJ002) of ADMC, with the play burst signal, and then performing edge detection at IC5 and 6. The output of edge detection is the C-TRIG signal. This is input to IC2 — 17P and triggers FF in IC2 to output the C-INC signal from 60P which acts as the 140nS shift circuit control signal.

The C-INV signal is then input to IC103 — 9P of DAPS where switching to activate and deactivate 140nS delay is performed.

3.3.3. RAM Control IC (PDJ002)

The CLD-3030 incorporates the PDJ002 as its RAM control IC. This IC differs from the PD3080 employed in the LD-S1 in the following ways.

< Additional functions not performed by the PD3080 (in VMRB of LD-S1) >

1. V-SYNC separation for REF-C-SYNC, MMV for half H rejection
2. Phase comparator for 1152fH VCXO drive
3. Burst extraction for D/A converted video signal

< Other functions >

1. Control signal generation (WRS, CE, RE) for D-RAM (MN4700)
   Address signal generation (A0 — A14) for D-RAM (MN4700)
2. Clock for D-RAM, A/D converter, D/A converter (SCK, LTCK, DACK)
3. Phase comparator to check burst continuity in the D/A converted video signal
   Two 3.58M signals are derived by frequency dividing the 4fsc signal by 4 and then shifting signal phase by 90°. These signals are then compared with the burst signal and output as P-DET1, 2.

The video memory section is composed of the two circuit boards, ADMC and DAPS.

3.3.4 Writing Data to RAM

Sampling of the video signal is done at 576fH (=9.06M) just as in the LD-S1 with 8-bit quantization. Data recorded in RAM has 512 samples on the H axis and 256 on the V axis which means that RAM capacity required is the same as for the LD-S1, namely:

$8 \times 256 \times 512 = 1048576$ (bits).

In the CLD-3030, one chip of RAM (MN4700) has the capacity to handle this volume of data.

First of all, the 8-bit parallel data from the A/D converter is divided into an upper and lower 4-bits. Because the D-RAM (MN4700) employed in the CLD-3030 has been specifically designed for video memory applications, it has separate 4-bit data buses for write and readout.

As the figures to the right show, data is sent in 4-bit increments, the upper 4-bits first and then the lower 4-bits, to RAM.

Furthermore, the MN4700 is equipped with an 8-bit serial shift register that can realize 8-bits of information for each bit input to the 4-bit data bus.

The 8-bit register is transmitted in sequence and when all 8-bits are assembled they are sent to the memory cell to complete recording to memory.

Because 8-bit serial data processing is being employed, one line of the 4-bit data bus, in fact, yields a total of 32-bits. In other words, one block of data handled by the system is equivalent to 4 samples.

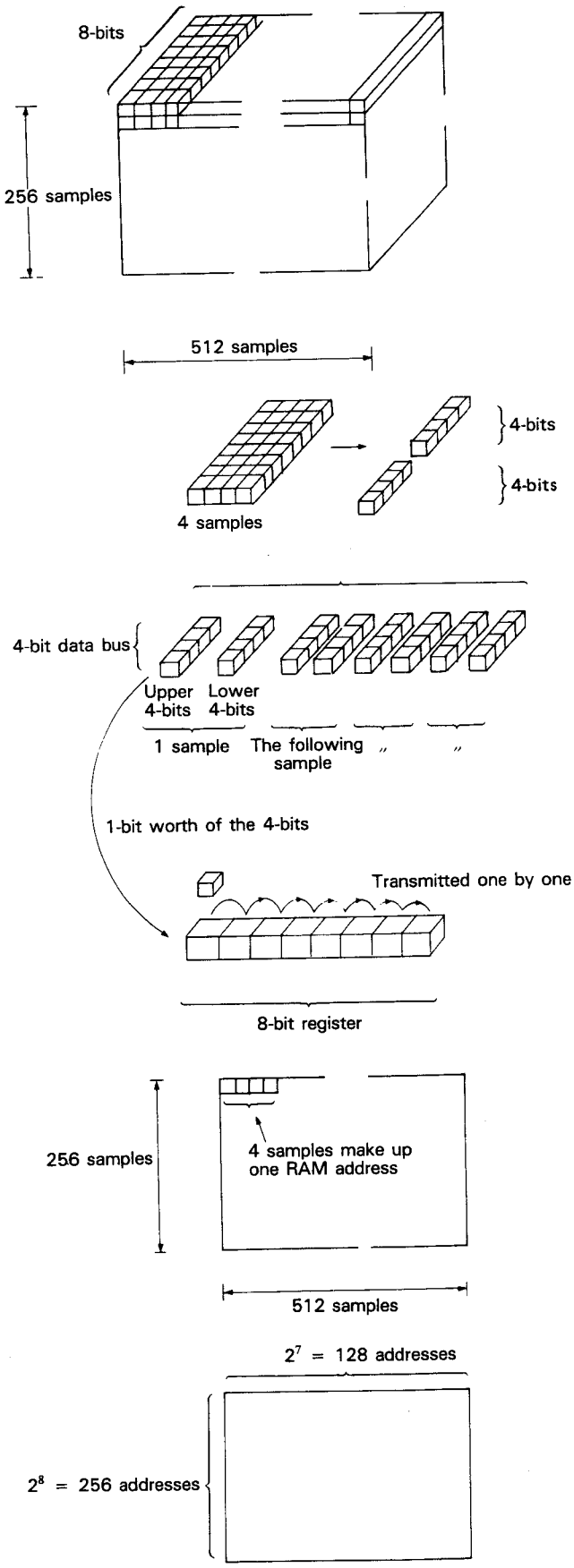
In order to arrange and process 4 samples worth of data (=32 bits) in RAM, one RAM address corresponds to 4 samples worth of data. Consequently, the number of RAM addresses required is:

H axis: $512/4 = 128 = 2^7 = 7$-bits

V axis: $256 = 2^8 = 8$-bits

Total bits required = 15-bits.

Because the MN4700 does not employ the address multiplexing normally found in D-RAM which allows switching between row and column addresses, it inputs the addresses as 15bit data.



<Data Processing in RAM>

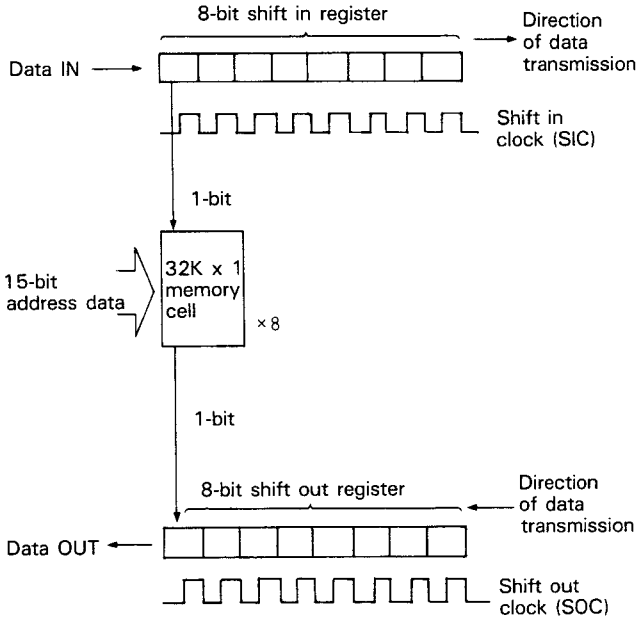
The figure to the right shows one bit worth of data from a 4-bit data bus. Each 8-bit register is connected to a 32K-bit memory cell and in RAM there are a total of 8 × 4 = 32 of these 32K-bit memory cells yielding a memory storage capacity of

32,768 × 32 = 1,048,576.

Because of the need to process the 8-bit data sampled at 576fH in 4-bit units, the frequency of the shift-in, shift-out clock has been set at

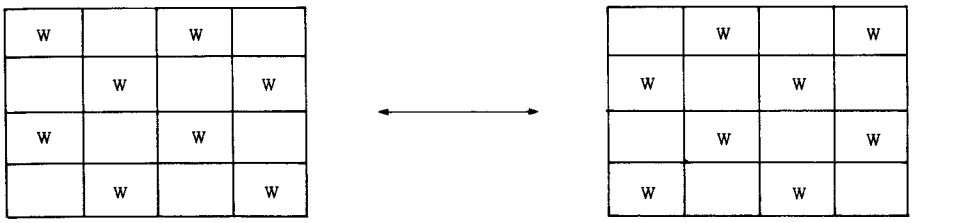
576 × 2 = 1152fH (=18.12M).

The necessary clock and timing signals needed for the operation of MN4700, as well as data I/O are all input from the RAM control IC, PDJ002.



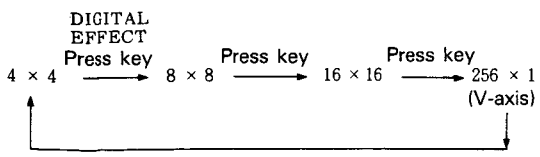
3.3.5. How Digital Effects Work

During strobe play, the unit goes into a partitioned screen mode. When the key is pressed once, the following operation occurs "W" is the area to be written to memory).



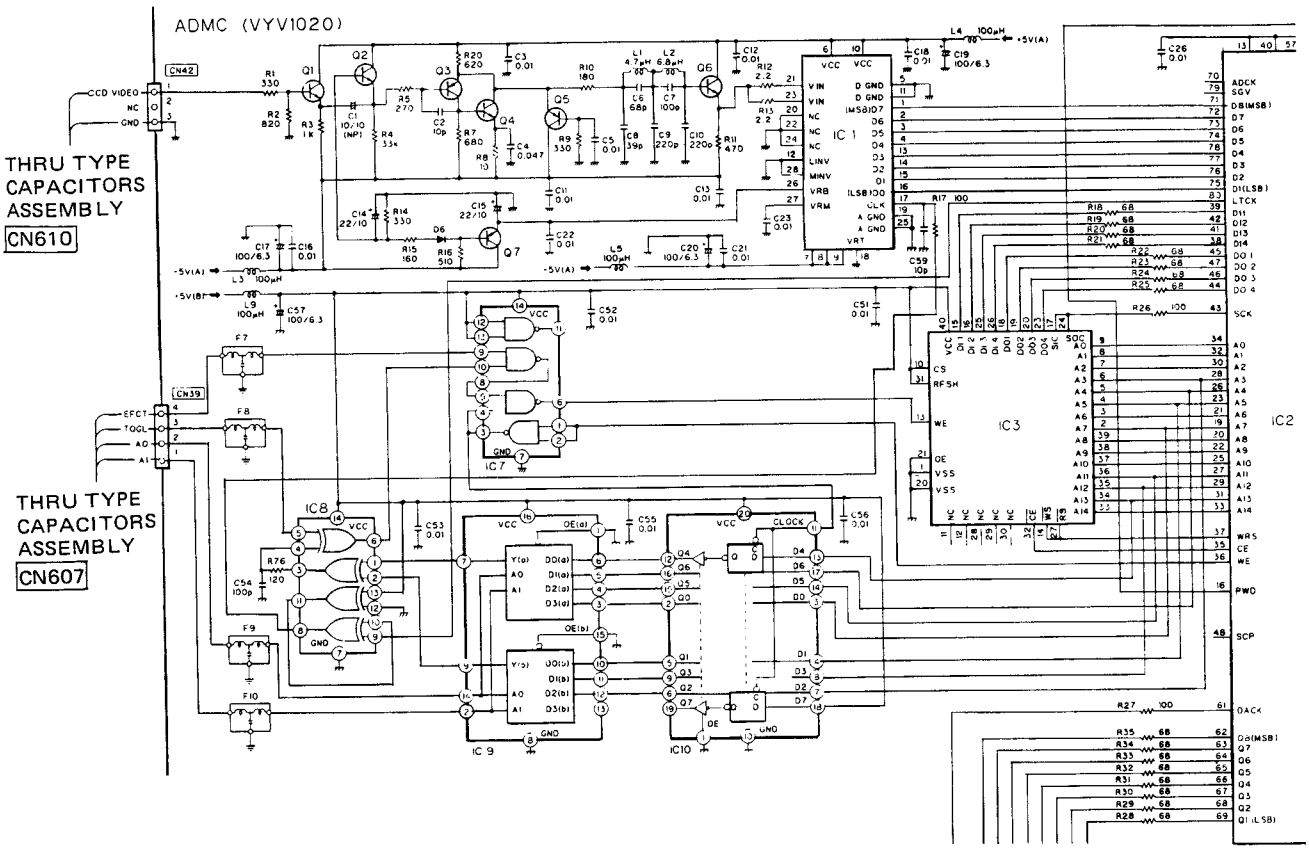
The screen is partitioned into a 4 × 4 Pattern with 16 boxes as shown above. 8 boxes at a time are alternately written to memory. Write speed at this time is the same as for normal strobe play, i.e. set to 1/4 at power ON, and variable with the remote control +, − speed KEY from 1/2 to STEP 3 (from every 2 frames to every 3 seconds).

The result is the special effect achieved on screen by shifting the write speed timing for the neighboring areas. Continuing to press the DIGITAL EFFECT key one or more times, alters the screen by increasing the number of partitions as shown in the figure below.



During these operations, the chroma signal and color burst phase for the neighboring areas must coincide. Since the phase of the burst signal is reversed for each frame, the phase for every other frame will be the same. That's why the DIGITAL EFFECT write speed is limited to integral multiples of 2 and can only be performed during strobe play.

3.3.6. Operation of the DIGITAL EFFECT INTERFACE



IC10 latches WRITE ADDRESS DATA.
When the WE signal of IC3 — 13P is L, the RAM WRITE/READ switch is on WRITE. From IC2 — 36P, the WE signal passes through two NAND gates in IC7 and is input to IC3 (RAM) — 13P and the WE signal which has been inverted once is input to IC10 — 11P (CLOCK pin).

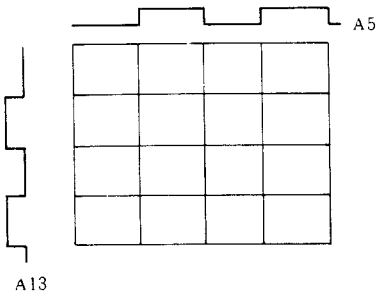
Since IC10 latches input data on the leading edge of the CLOCK pulse and sets the L to H, i.e., READ to WRITE, timing, it can latch WRITE ADDRESS.

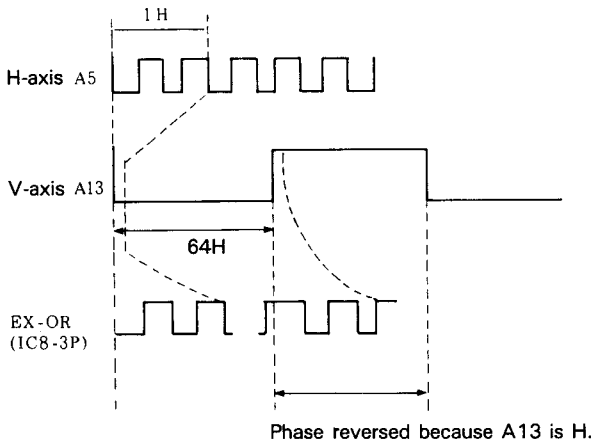
IC9 acts as an address selector for setting the number of screen partitions during DIGITAL EFFECT. Of the four possible choices, the number of screen partitions selected is determined by the A0 and A1 signals generated by the system microprocessor CPU as follows.

A0	A1	Selected address	Number of screen partitions
L	L	A5 A13	4 x 4
H	L	A4 A12	8 x 8
L	H	A3 A11	16 x 16
H	H	A7	256 x 1

Next, two addresses are input to EX-OR. This takes the data from the partitioned screen and writes it in alternating form to memory and, depending on whether the V axis address data is L or H, reverses the H axis address data. The next EX-OR has a switching function. On the basis of the TOGL signal generated by the system microprocessor CPU, it does or does not perform inversion one more time.

The 4 x Partitioned screen is taken as an example here.





Phase reversed because A13 is H.

Then the output of IC8 — 3P is input again to EX-OR.

When the TOGL signal generated by the system microprocessor CPU and input to the second EX-OR is L, polarity remains unchanged and the video signal is output from 6P as is. On the other hand, if TOGL is H, the signal is inverted and then output from 6P.

If IC7 — 9P is H when DIGITAL EFFECT is ON, the output of IC8 — 6P is inverted before being input to the NAND gate.

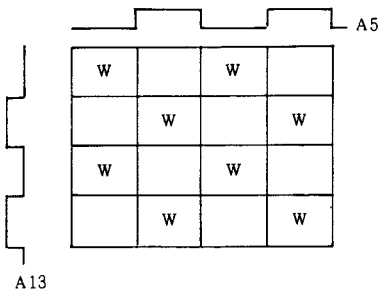
Another input to the NAND gate is the inverted WE signal from the RAM control IC (IC2). This allows WE to be controlled by the output of IC8 — 6P. In other words:

When IC8 — 6P is L: The WE signal from IC2 is input to IC3 (D-RAM) — 13p, WE pin.
WRITE to memory is performed.

When IC8 — 6P is H: The WE signal from IC2 is not input to IC3 - 13P and because it is H, nothing will be written to memory.

Furthermore, as the figure below shows, the L or H of TOGL indicates which areas (shown by W) of the screen are to be written to memory.

TOGL:L



W		W	
	W		W
W		W	
	W		W

TOGL:H

	W		W
W		W	
	W		W
W		W	

4. DIGITAL AUDIO CIRCUITRY

4.1 SUMMARY

The 4FSB circuit board receives the EFM signal from the VDEM section of the VSOP Assembly and performs the necessary signal processing. The principle IC for this purpose is the CXD1135Q, which has the following functions:

1. Generation of the bit clock (PLCK: 4.3218M) by EFM-PLL
2. EFM signal demodulation, correction and interpolation
3. Frame synch signal detection, protection and interpolation
4. Subcode signal demodulation and error detection
5. SPDL servo (obligatory deceleration/acceleration, brake, speed servo, phase servo)
6. Zero cross counter for 8-bit tracking error (not found in these models)
7. Double oversampling digital filter (35-stages)
8. Digital audio interphase output

The functions listed in 1 — 6 are essentially those handled by the CX23035 found in previous models. Both the CXD1135Q and the CX23035 receive commands from the system microprocessor in the form of 8-bit serial command data and, in terms of the CX23035 commands, the CXD1135Q is upward compatible.

4.2 CXD1135Q COMMAND CODE

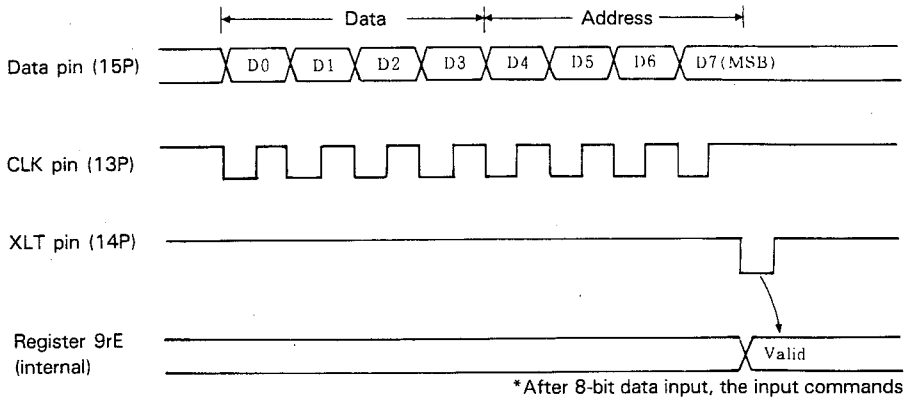
As the table below shows, CXD1135Q has a 4-bit register containing addresses 9 through E. Player operations can be performed by sending 8-bit data (command code) containing address and data (totalling 8-bits) to these addresses.

<Register Chart>

Register Name	Command	Addresses D7 – D4	Data				SENS pin (18P)
			D3	D2	D1	D0	
9	Control of new functions	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A	Synch protection, attenuation control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Lower 4-bits	1011	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set, Upper 4-bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT
D	CLV control	1101	DIV	Tz	Tp	GAIN	Z
E	CLV mode	1100		CLV mode			Pw≧64

* The B.C register is for tracking error zero cross count and is not employed in the 1988 models.

<Data Input Timing Chart>



*After 8-bit data input, the input commands are executed during the time period when XLT is L. Data input timing is the same as in the CXA1082A.

«Information about the Registers»

• Register 9

Register 9 handles the commands for new functions not found in the previously employed CX23035. Registers A through E, however, are essentially the same as in the CX23035.

		Dn = 0	Dn = 1
ZCMT	D3	Zero cross MUTE OFF	Zero cross MUTE ON
HZPD	D2	The PDO pin is always active	The PDO pin is Z at the trailing edge of GFS
NCLV	D1	CLV-P servo supported by frame synch signal	CLV-P servo supported by base count
CRCQ	D0	CRCF is not superimposed on SUBQ	At the leading edge of SCOR, SUBQ = CRCF
		(Functions identical to those of the CX23035)	(New functions)

ZCMT: Turns zero cross MUTE ON/OFF.

HZPD: Switches PD output to Hi-Z (ON/OFF) from the trailing edge of the GFS pulse (GFS is H when SPDL LOCK is activated) to a maximum of 0.55nS. (PLCK and play EFM undergo phase comparison, and the PD output controls the VCO.)

NCLV: Switches the SPDL phase servo error detection method when PLL is locked.

CRCQ: Switches the output of CRCF data from the subcode data Qoutput pin, SUBQ, ON/OFF.

If the content of Register 9 is cancelled out by activating POWER ON RESET and none of its commands are active, the IC will function exactly like the CX23035.

• Register A

Controls the 4 signals: GSEM, GSEL, WSEL, ATTM.

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

When frame synch detection is not working properly, a dummy frame synch is interpolated, but the number of frames for which interpolation will be performed is fixed: during LD play, 8 frames; during CD play (CLD-3030, CLD-1030) 8 frames; and during SCAN, 13 frames.

WSEL	Clock
0	± 3
1	± 7

To prevent errors during frame synch detection, a detection window of a certain width is set and synch patterns which fall outside the detection window are ignored. The width of the detection window is set as follows: (set at ± 7 clock)

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

In combination with the MUTG pin (19P), MUTE ON/OFF and the application of -12dB attenuation can be controlled.

In terms of actual command code, $AA is being input. Since A = 1010 and GSEL = 1, GSEL = 0, there are 8 interpolation frames with detection width parameter set at 7 clock.

• **Register D**

DIV	D3	0	RFCK/4 and WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 and WFCK/8	
TB	D2	0	RFCK/32	Bottom hold cycles in CLV-S, CLV-H modes
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold cycle in CLV-S mode
		0	RFCK/2	
GAIN	D0	0	− 12dB	MDP pin gain in CLV-S, CLV-H modes
		1	0dB	

RFCK: Read Frame Clock (frequency divided from X'TAL, 7.35k)

WFCK: Write Frame Clock (Frame synch during play EFM)

CLV-P mode: Phase servo which operates when the PLL loop is locked

CLV-S mode: Speed servo which operates when the PLL loop is not locked

CLV-H mode: Speed servo during search (when pickup is moving)

In terms of actual command code, $D4 is being input. Since 4 = 0100, RFCK, WFCK are frequency divided by 4 for phase error, RFCK is frequency divided by 16 for bottom hold in the CLV-S mode, RFCK is frequency divided by 4 for peak hold and MDP pin gain is − 12dB.

• **Register E**

		(3P)	(4P)	(1P)	(2P)
Mode	**D3–D0**	**MDP pin**	**MDS pin**	**FSW pin**	**MON pin**
STOP	1000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	Z	L	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H
CLV-A'	0101	CLV-S' or CLV-P	Z or CLV-P	L or Z	H

This register sets the operating mode for the SPDL servo. In this mode, the SENS pin, 19P, registers L when the frame sync pulse amplitude detected at CLV-S is over 64T. This output, however, is not utilized.

From commands 0000 to 0110, the system is identical to that of the CX23035.

After the focus servo lock check, actual SPDL start is performed by $E8, i.e., command code 1000 puts the unit into KICK mode which force starts the SPDL. Next, $E6 puts the unit into CLV-A mode which closes the SPDL servo and PLL loop. The lock can be checked by verifying that GFS registers an H.

When stopping, $EA, command code 1010, applies the brake, and after SPDL stop detection at FG, $EO puts the unit into stop mode. Because the CD-3030 has a 4-times oversampling digital filter IC (SM5807B), the digital filter in the CXD1135Q is not utilized.

As a digital OUT terminal, the toss link for optical fiber transmission (identical to that of the D-1000) is passed through a buffer and connected to 27P. However, since the function assigned to MODE 0 of the digital OUT IC, CX23033, employed in the D-1000 is built into the CXD1135Q, 27P is no longer needed for this purpose. Instead, modulated output for the digital audio interface format is obtained from 27P.

ON/OFF for digital filter and OUT functions can be fixed according to the H and L signals from MD1, 2 and 3 of 55, 56 and 57P. On the CD-3030 these are set at L, L, H corresponding to digital, OFF and digital OUT, ON.

4.3. SIGNAL PROCESSING AND CXD1135Q PERIPHERAL CIRCUITRY

The EFM signal from the VDEM section of the VSOP Assembly passes through the ATC circuit made up of IC101 (TC40H004P) and IC102 (1/2) (NJM082D) and is input to IC104 — 5P (CXD1135Q). The result of phase comparison between EFM and the VCO output of IC102 (2/2) is output from IC104 — 11P. A PLL loop is used to control a VCO.

IC104 performs SPDL servo error detection from EFM and the output of 1 through 4P is utilized for the SPDL servo. The function of the pins is as follows:

FSW (1P): When the PLL loop is locked, it is Hi-Z. At other times it is L.
IC103 (2/2) (NJM082S) is the phase and speed error mix filter, and is used to switch the cut-off frequency. (Hi-Z, 500Hz, L: 20Hz).

MON (2P): When the motor is stopped: L, when rotating: H.

MDP (3P): SPDL phase error when PLL is locked and otherwise, speed error

MDS (4P): Speed error when PLL is locked and, otherwise, Hi-Z

Internal detection of whether PLL is locked or not, is performed at the GFS pin, 28P, which registers H when PLL is locked.

During CD play or the audio section of a CDV, the error signal of IC103 — 8P is input as CD ERR to the absolute value amp for the SPDL servo section from IC501 — 15P (NJU4053BD) and drives the SPDL motor.

During LDD play or the video section of a CDV, a 384fs (= 16.9344M) VCXO is input IC501 — 4P to control VCXO. As a clock signal, VCXO is input to IC104 and IC201 (SM5807B). At IC104 the demodulated digital audio data is input as serial data to IC201 along with LRCK (44.1k) and C210 (2.1168M).

IC201 is a 61-stage + 13-stage 4-times oversampling digital filter.

The CLD-3030 utilizes a sub-CPU, IC106 (PDE0234), to handle the transmission of 8-bit serial command data to IC104 (CXD1135Q) and the reception of sub-code data from IC104.

IC106 is connected to the main CPU by the 4-bit data bus and by the signal lines ATN, STB and ACK. PD0031 and PDG012 are also connected to the data bus.

The CLD-1010 does not use a CPU. Instead the decoder ICs (CX23035, CXD1135Q) are controlled directly from the main CPU and data I/O is performed.

In previous models, the only operation using sub-code data during LDD play was the Emphasis ON/OFF check. This helped keep processing time short and allowed the main CPU to directly read data.

However, with the introduction of TOC (ADR = 4) in LDD discs, the reading of the TOC renders processing time too long and it is no longer practical for the main CPU to directly read the data.

For this reason, sub-code data from CXD1135Q is placed in a buffer at IC106 (PDE024) and, in response to a command from the main CPU, is transmitted by 4-bit bus. In addition, command code destined for CXD1135Q is input through IC106.

On the basis of data received from CXD1135Q and the main CPU, IC106 performs digital/analog switching, LD/CD switching and Emphasis ON/OFF.

Another function of IC106 is to output LSEL and RSEL signals used for switching left/right channels during LDD play:

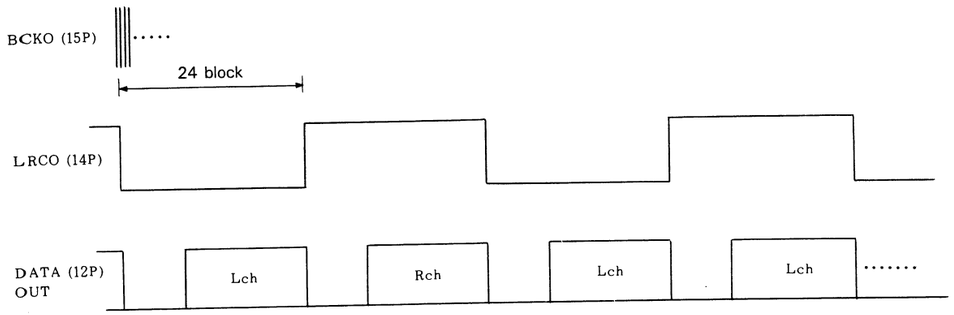
	Both CH	RCH only	LCH only
LSEL	L	L	H
RSEL	L	H	L

As the figure on the facing pages shows, Lch, Rch data is output in alternating form from IC201 (SM5807B). L/R switching during LDD play and L-R, same phase D/A conversion during normal play are performed at IC202, 203 and 204. (L.R. same phase conversion is performed at PD-7070.)

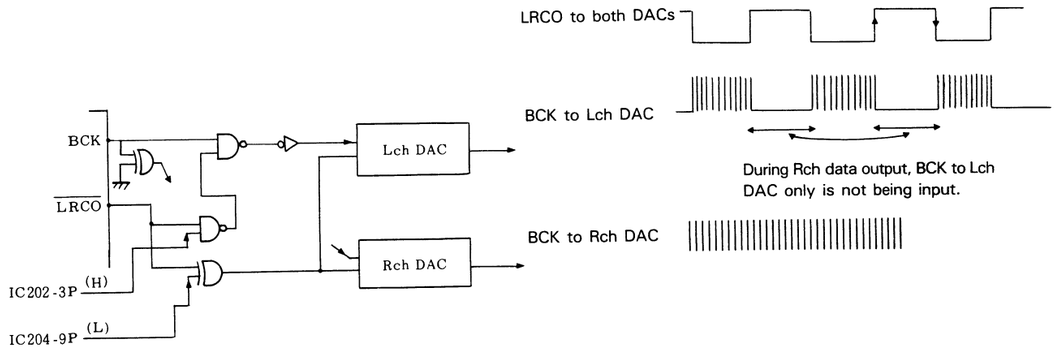
Next, the timing for L/R switching is shown.

4.4. THE L/R SWITCHING SYSTEM FOR DIGITAL AUDIO

IC201 (SM5807) Output



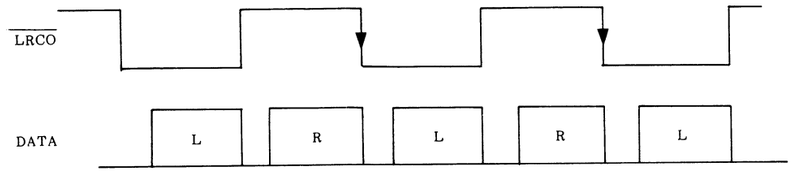
① When both L,R are output (LSEL = L, RSEL = L)



In this mode, LRCO is H for the Lch DAC and DATA BCK, which means that input to DAC is halted while Rch data is being output. Since both DACs are latching and outputting data on the trailing edge of LRCO, L and R are being output simultaneously on the trailing edge of LRCO.

② Rch only output (RSEL only = H)

When RSEL is H, IC204 — 5P also outputs an H. Since IC204 — 9P is L, IC203 — 11P becomes H and IC202 — 3P becomes L. As a result, IC202 — 11P becomes H and BCK to the Lch DAC is not gated to LRCO but continues being input.

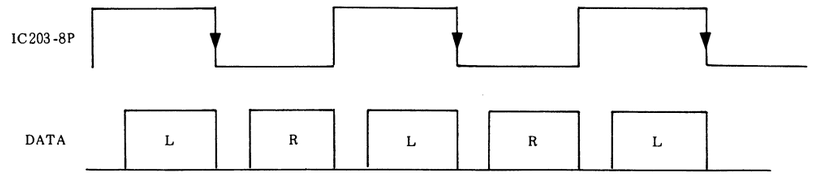


Because IC204 — 9P is L, LRCO is input to both DACs without undergoing phase reversal.

Consequently, since both DACs are latching data on the trailing edge of LRCO, only Rch data is being output by the DACs.

③ Lch only output (LSEL only = H)

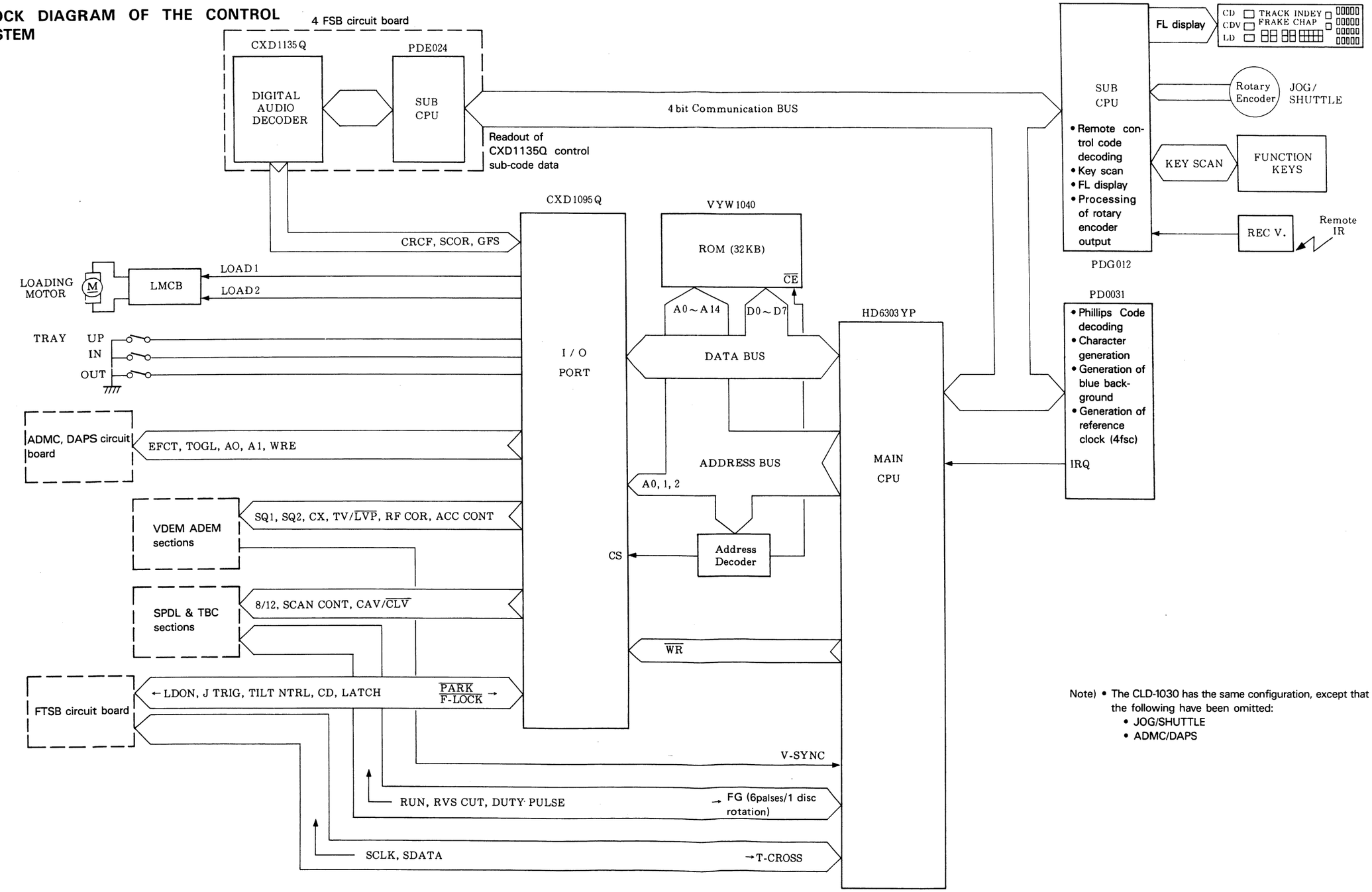
When LSEL is H, IC204 — 9P also outputs an H which inverts the LRCO for both DACs. Since IC204 — 5P is L, IC202 — 11P becomes H and the BCK to the Lch DAC is not gated.



Consequently, since both DACs are simultaneously latching Lch data, Lch audio is output from both DACs. DAC output then passes through the 3-stage LPFs, IC207, 208.

5. EXPLANATION OF SOFTWARE USED IN THE SYSTEM MICROPROCESSOR

5.1. BLOCK DIAGRAM OF THE CONTROL SYSTEM



Note) • The CLD-1030 has the same configuration, except that the following have been omitted:
- JOG/SHUTTLE
- ADMC/DAPS

5.2. THE ICS IN THE CONTROL SYSTEM

HD6303Y: is an externally connected ROM-type 8-bit CPU and operates on the basis of the program written to the externally connected ROM.

PDG012: is a 4-bit CPU which performs JOG/SHUTTLE decoding, main unit key decoding, remote control key decoding and maintains FL, LED displays on the main unit.

PDE024: is a 4-bit CPU which performs LDD control. It performs sub-code decoding and controls CXD1135Q.

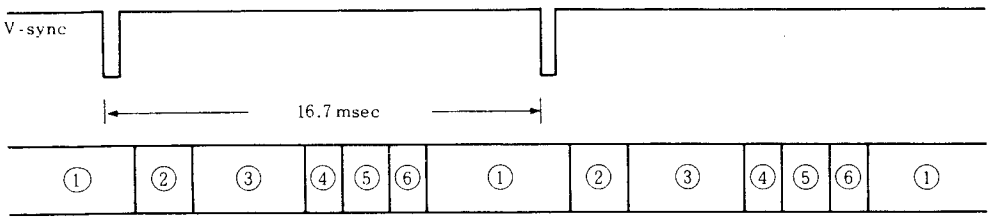
CXD1095Q: is an enlarged I/O port IC connected to HD6303Y of the main CPU.

MBM27C256: ROM (32k) contains the program for HD6303Y.

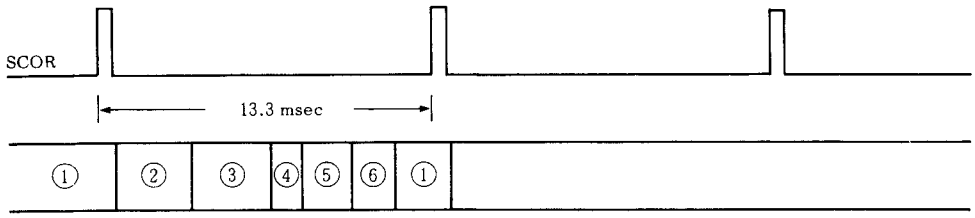
5.3 SUMMARY

The main CPU, HD6303Y, reads code, handles displays and key information and performs all control functions, including servo control, loading, etc. The processing routine is arranged in a loop with time division for processing handled by an internal timer and play synch signal. When the unit is in the LD mode, the internal timer is set to 20msec and, if the play V-synch signal doesn't intervene, the signal covers the loop in a period of 20msec. When time division is applied from the play V-synch signal, the internal timer is reset and the period for covering the loop is equal to the V-synch period of 16.7msec.

When the unit is in the CD mode, the internal timer is set to 20msec and, if sub-code data doesn't intervene, the signal covers the loop in a period of 20msec. If subcode data is applied, timing is reset and the period for covering the loop is equal to the SCOR period of 13.3msec.

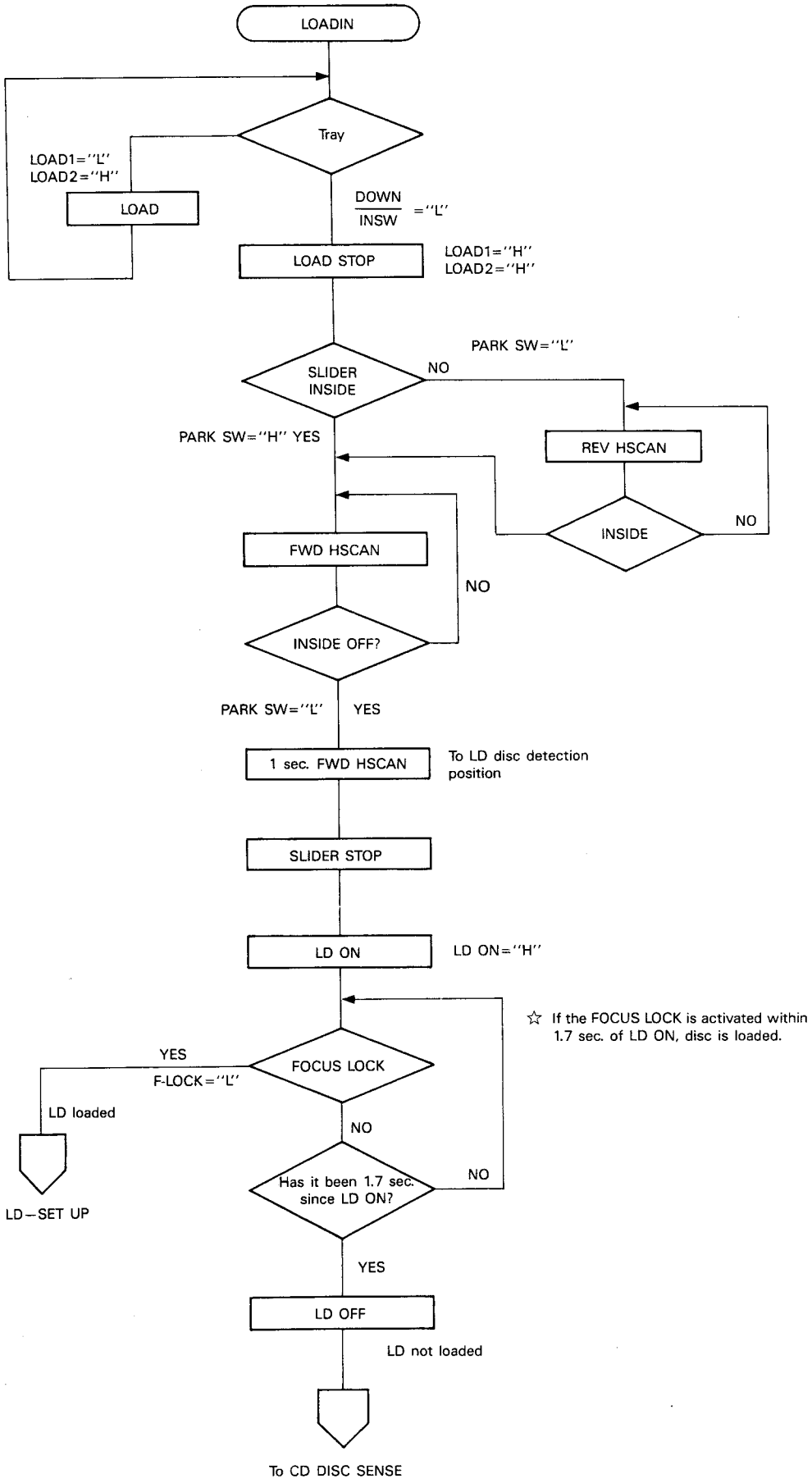


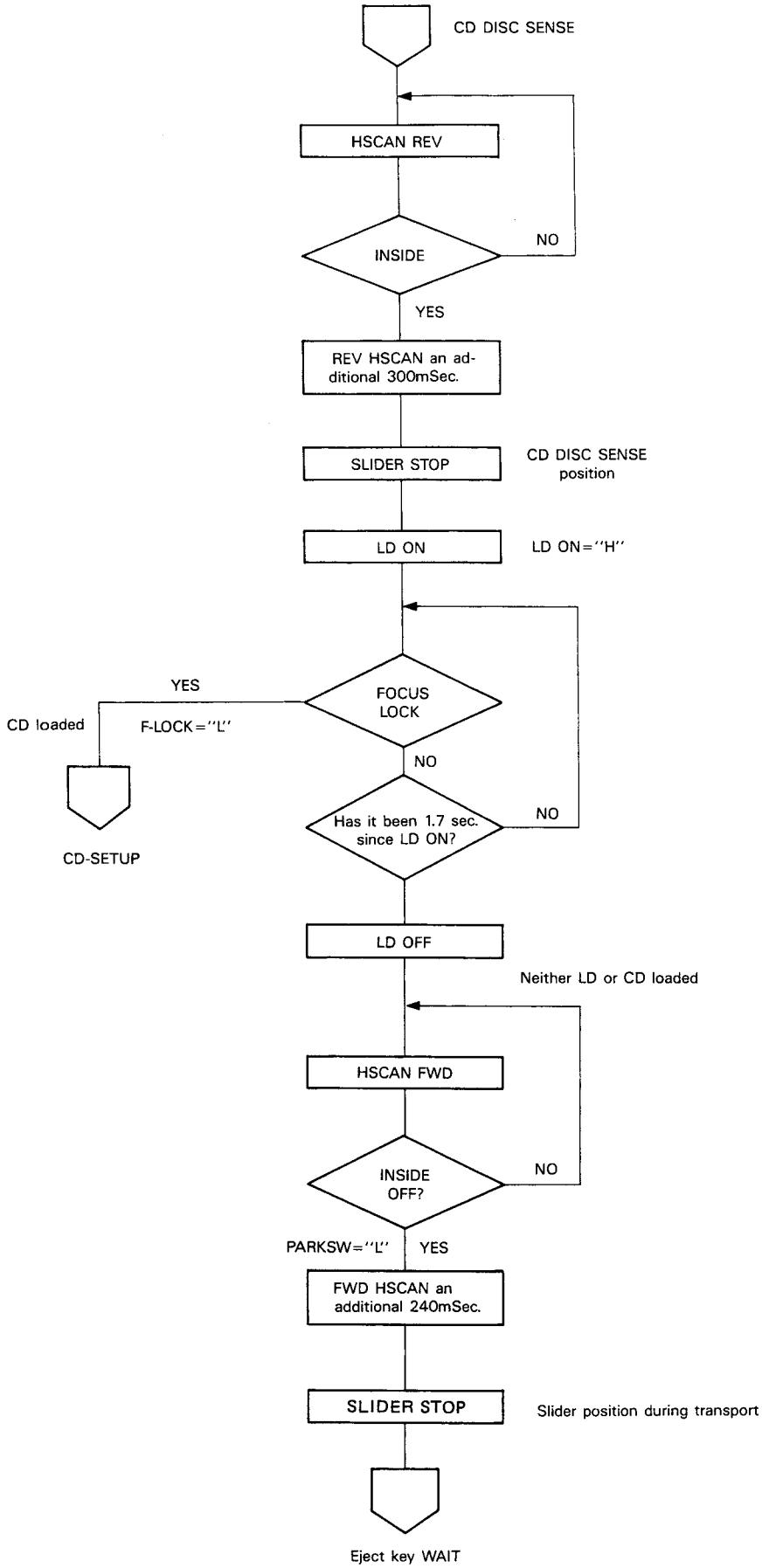
① V-sync WAIT and jump control
② Code readout
③ Display control
④ Key readout and processing
⑤ Servo and mechanical control
⑥ Backup, audio control

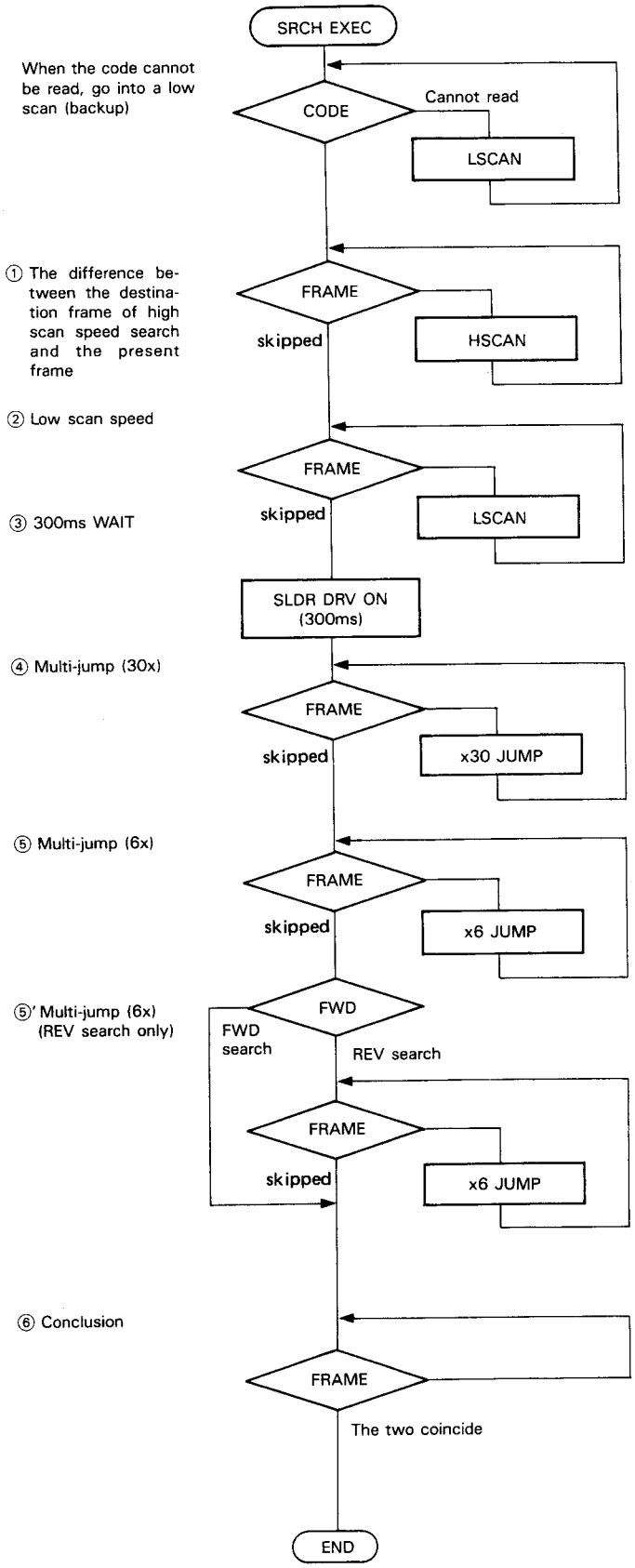


① Sync WAIT
② Subcode readout
③ Display control
④ Key readout and processing
⑤ Servo and mechanical control
⑥ Backup

Fig. 5-3-1. Control Summary Timing Chart


LOADIN
Tray
LOAD1="L"
LOAD2="H"
LOAD
DOWN / INSW ="L"
LOAD STOP
LOAD1="H"
LOAD2="H"
PARK SW="L"
SLIDER INSIDE
NO
PARK SW="H" YES
REV HSCAN
INSIDE
NO
FWD HSCAN
NO
INSIDE OFF?
PARK SW="L"
YES
1 sec. FWD HSCAN
To LD disc detection position
SLIDER STOP
LD ON
LD ON="H"
☆ If the FOCUS LOCK is activated within 1.7 sec. of LD ON, disc is loaded.
YES
F-LOCK="L"
FOCUS LOCK
LD loaded
NO
Has it been 1.7 sec. since LD ON?
NO
LD—SET UP
YES
LD OFF
LD not loaded
To CD DISC SENSE


CD DISC SENSE
HSCAN REV
INSIDE
NO
YES
REV HSCAN an additional 300mSec.
SLIDER STOP
CD DISC SENSE position
LD ON
LD ON="H"
FOCUS LOCK
YES
CD loaded
F-LOCK="L"
CD-SETUP
NO
Has it been 1.7 sec. since LD ON?
NO
LD OFF
Neither LD or CD loaded
HSCAN FWD
INSIDE OFF?
NO
PARKSW="L"
YES
FWD HSCAN an additional 240mSec.
SLIDER STOP
Slider position during transport
Eject key WAIT


SRCH EXEC
When the code cannot be read, go into a low scan (backup)
CODE
Cannot read
LSCAN
① The difference between the destination frame of high scan speed search and the present frame
FRAME
skipped
HSCAN
② Low scan speed
FRAME
③ 300ms WAIT
skipped
LSCAN
SLDR DRV ON (300ms)
④ Multi-jump (30x)
FRAME
skipped
x30 JUMP
⑤ Multi-jump (6x)
FRAME
skipped
x6 JUMP
⑤' Multi-jump (6x) (REV search only)
FWD
FWD search
REV search
FRAME
skipped
x6 JUMP
⑥ Conclusion
FRAME
The two coincide
END

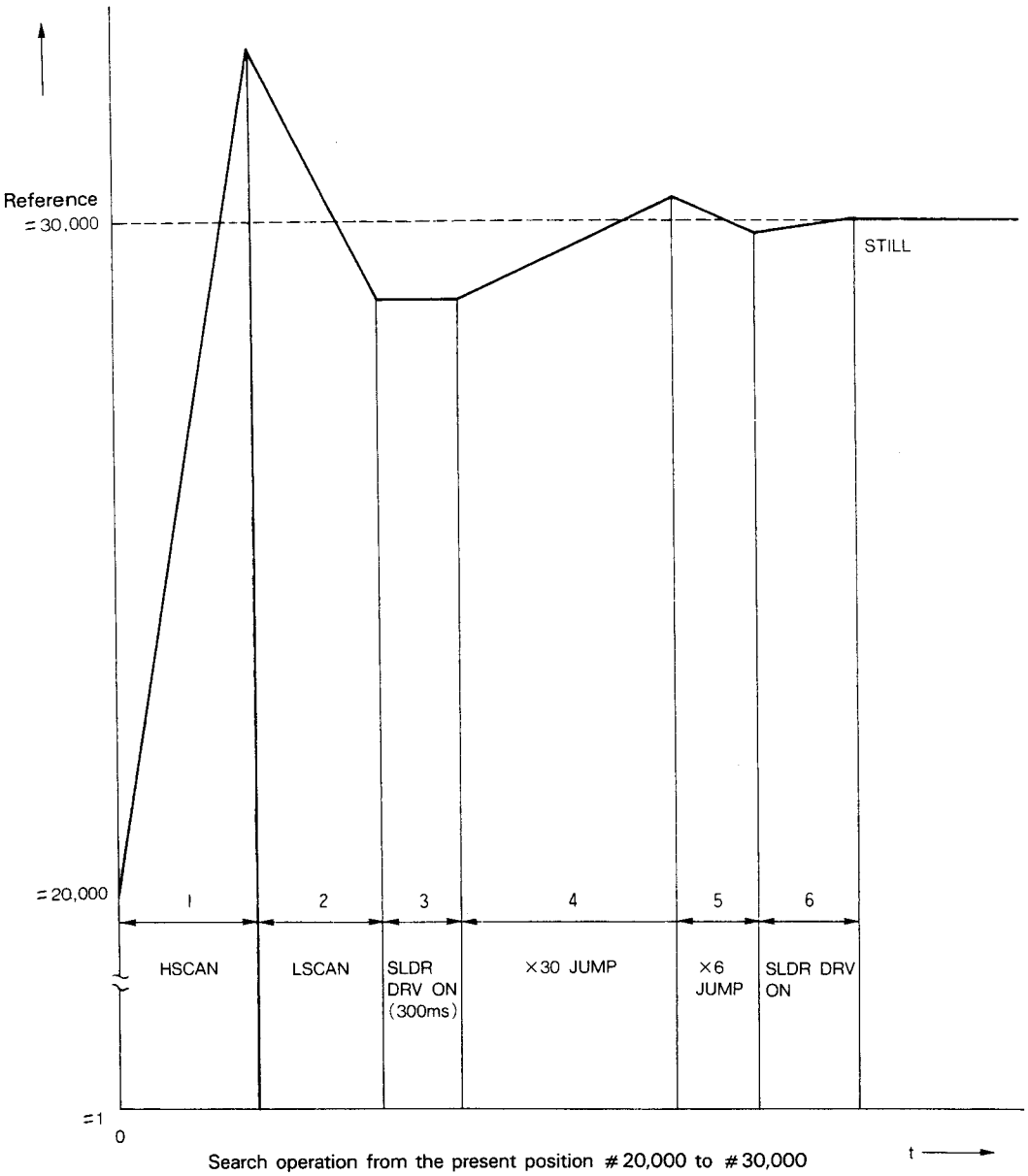


Fig. 5-3. Frame Search Operation

5.4. THE CONDEPT BEHIND SPECIAL PLAY OPERATIONS

An explanation of the basic concepts behind the special play operations incorporated in the CLV disc.

5.4.1. STILL Operation

When the STILL key is pressed, the disc rotates twice and the operation is complete.

Based on the spindle motor derived FG signal which registers disc rotations, the CPU counts Pulses of the FG signal (1 rotation = Pulses) to determine that the disc has made a half rotation, and then the CPU converts the signal to the ROTATION (ROT) signal.

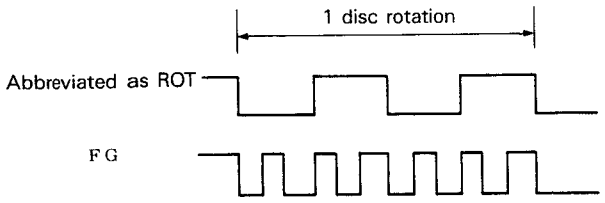


Fig. 5-4-1.

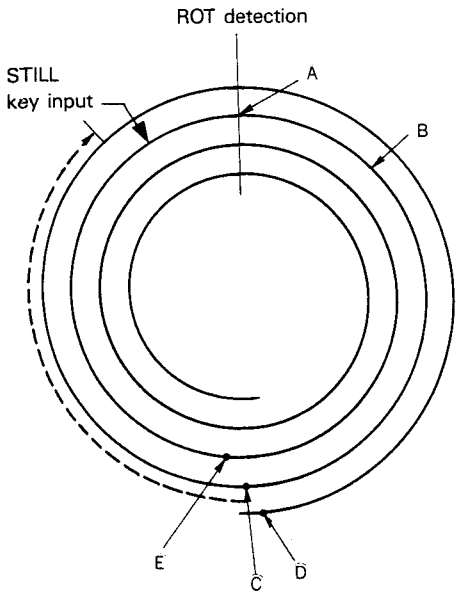


Fig. 5-4-2.

1. The STILL key is pressed.
2. When the ROT signal is detected at point A , the CPU puts V-SYNCH on INPUT WAIT.
3. At point B V-SYNCH is detected but the CPU is still waiting with the next V-SYNCH input.
4. When V-SYNCH is input at point C , the CPU immediately outputs a WRITE ENABLE signal to video memory and from point C one frame worth of signal is input to memory (indicated by the dotted line that begins at point C).
5. The disc then makes a single rotation and after V-SYNCH detection at point D and readout of Philips code are performed, a two track reverse jump is made (interval of 1msec) to point E .
6. Return to Step 2 above and repeat the operation.

This explains, then, in brief, how the STILL operation is completed in the interval of two disc rotations.

5.4.2. STEP Operation

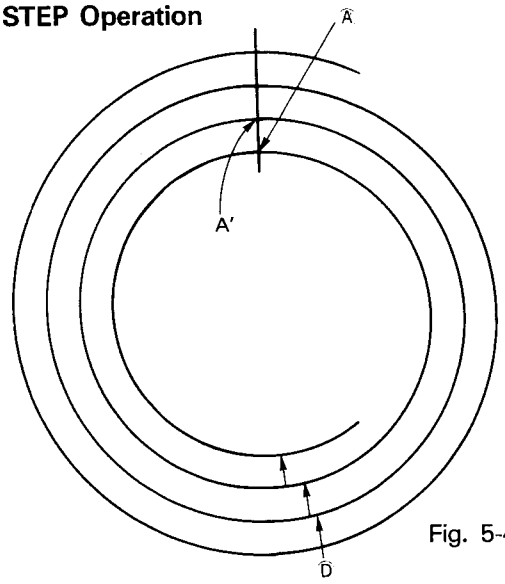


Fig. 5-4-3.

As Fig. 5-4-3 shows, in the STILL mode described above, the two track reverse jump from point D and the return to point A are repeated. At that point however, if a one track reverse jump only is performed from point D , the pickup is one track later or further out from point A on the ROT detection spot at a point we call A '.

If a normal STILL operation is then performed from point A ', the field that is written to memory will be slightly different from the first field. This maneuver is what makes the STEP FWD operation possible.

Conversely, if a three track reverse jump is made from point D this will put the pickup one track earlier than the first field written to memory and during playback there will be a STEP REV effect.